MODULATION EFFECTS ON ORGANIC ELECTRONICS

A Thesis
Presented to
The Academic Faculty

by

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In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy

School of Chemistry and Biochemistry
Georgia Institute of Technology
December 2005

MODULATION EFFECTS ON ORGANIC ELECTRONICS

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To My Wife ,

My Father ,

My Mother

and

My Baby Daughter

ACKNOWLEDGEMENTS

I feel it the greatest honor to express my sincerest thanks to my advisor, Professor Jiří Janata, and Dr. Mira Josowicz for their unwavering support and guidance throughout my graduate studies. I would also like to thank Professor Andrew Lyon, Professor John Z. Zhang and Professor Bernard Kippelen for serving on my thesis advisory committee.

I am grateful to Dr. Januz Kolewa at Georgia Institute of Technology and Dr. Karin Potje-Kamloth at Institut für Mikrotechnik Mainz GmbH, Germany for providing the P3HT and PAMOP precursor sample. I would also like to thank for their valuable suggestion for my research.

I would like to thank my unfailingly pleasant and interesting group members for their friendship and assistance. I would also like to thank Frederic L'Hereec, Arun Rambhatlab and Dr. James Zhou for fabricating device chips at MIRC.

I would like to thank my wife Lin Chen who unselfishly supported my research work and my parents who embody all that is best in humanity by their selflessness, dedication and integrity. Finally, I would like to thank my 7 month old daughter Iris R. Chen who has been giving me great comfort during my hard working time.

This work was funded by NSF CHE -9816017, NSF ENG -95874, NSF ECS -0327608.

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SUMMARY

The first chapter of this thesis describes the application of building high aspect ratio epoxy mask with Taiyo PSR4000BN for on-chip micro-cell electrochemistry. Thickness up to 200 μm and aspect ratio up to 16:1 have been achieved with this material. It is demonstrated that this material satisfies the mechanical and chemical requirements. Also a three-electrode system has been setup for electrochemistry in micro-cell on chip. Tests with Poly(phenylenesulfidephenyleneamine) (PPSA) show that it is possible to precisely tune the properties (Work function and resistance) of conducting polymer in micro-cells on device chip.

In the second chapter, a new test platform GT03 has been described. It has an innovated design that can be used either as IGFET or OFET. It facilitates the study of chemical modulation of the critical parts of organic electronics. It is demonstrated that chemical species can affect organic electronic properties on bulk, interface and electric contacts. The contact effect in organic electronic is an important but overlooked factor that affects the functionality of organic electronics. Neglecting contact resistance will bring errors in signal processing or data interpreting.

In chapter III, another test platform "interdigitated structure" (IDS) has been designed and fabricated to systematically study the contact resistance in organic field-effect transistor (OFET). Modified 4-point-probe measurements were performed with IDS on poly(3-hexylthiophene) (P3HT) based OFETs. This test protocol allows the separation of the contact resistance at drain and source electrode, and also the material bulk resistance. It is demonstrated that the contact resistance and material bulk resistance are actually modulated by the gate electric field, and drain contact resistance and bulk resistance has similar functional relationship and magnitude.

In the last chapter, two methods have been used to reduce the influence of oxygen

doping in P3HT based OFETs. Annealing can remove the oxygen trapped in the P3HT film. Encapsulation with PAMOP can effectively slow down the oxygen doping in P3HT OFET. A model of oxygen doping in P3HT OFET has been suggested to explain the experimental data. It is demonstrated that oxygen doping can affect all the resistance components in P3HT OFET.

CHAPTER I

HIGH ASPECT-RATIO EPOXY MASK FOR ON-CHIP MICRO-CELL ELECTROCHEMISTRY

1.1 Introduction

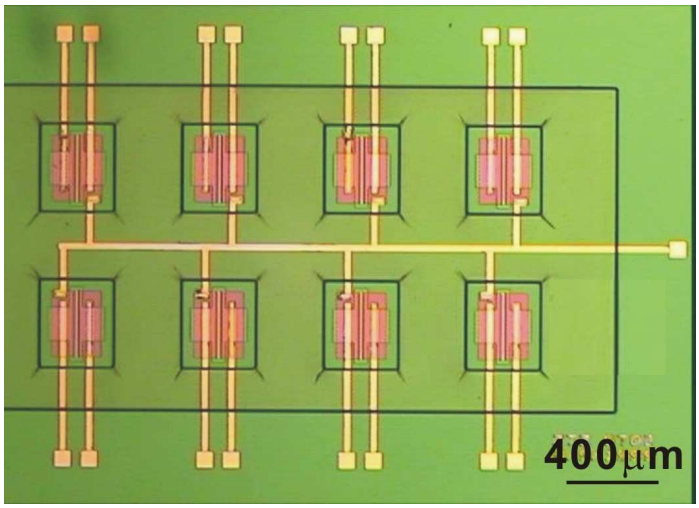
The history of chemical sensing can be traced back to very early days of human history. Modern chemical sensing techniques are developed based on the requirements to detect chemicals in hostile environments or inaccessible locations or when the compounds that need to be detected are toxic. Various chemical sensors have been designed and fabricated in many applications, in which they can provide the exact concentration of a compound with much higher sensitivity than "Natural" sensing.

A chemical sensor can be defined as a device which provides a continuous data stream about a chemical environment.[6] A Chemical sensor has two essential components, one is a chemically active material whose properties are altered when in contact with a compound of interest, the other is a transducer which measures chemical changes in the active material and converts that information into electrical signals.

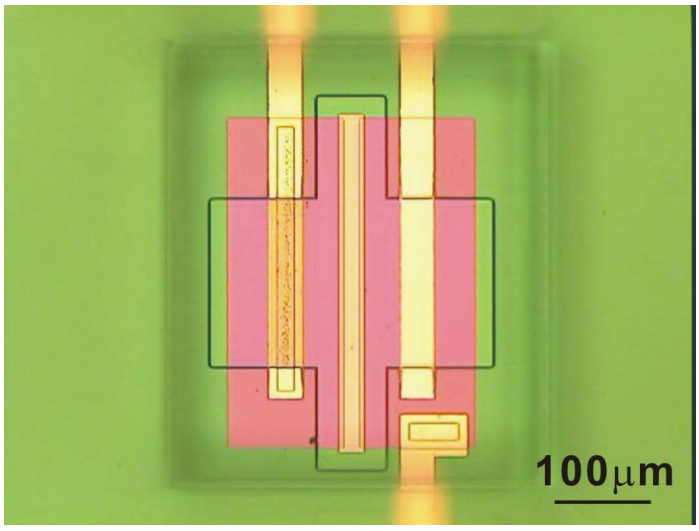
1.1.1 Fundamentals of chemical sensor array

Chemical sensors are increasingly used as arrays. Chemical sensor array can eliminate the interference from similar chemicals during the detection and quantification. Nowadays chemical sensor arrays have become important tools in many analyses such as: volatile analytes,[7] and online monitoring of biological liquids.[8] A chemical sensor array is usually made

up of a group of chemical sensors of same type, each chemical sensor uses a partially selective material to provide a pattern of response to a given chemical environment. Furthermore chemical sensor array takes the advantages of several different transduction principles to offer so called higher order sensing,[9] so the response pattern as a whole provide the desired 2-D or 3-D information about the analytes.



(a)



(b)

Figure 1.1: GT02 chemical sensor array chip with SU-8 epoxy mask separating individual ChemFETs. (a) GT02 chemical sensor array chip (b) A single ChemFET module on GT02 chip.

The concept, design and fabrication of a higher order chemical microsensor array GT02

have been described by Polk B. in 1999.[10] In this design shown in Fig 1.1, eight chemically sensitive field-effect transistors (ChemFETs) are built on a single chip, and two transduction principles are employed: chemical modulation of work function (WF) of sensing layers, and chemical modulation of impedance of the same sensing layer. When sensing layers are exposed to analytes (in this thesis, we are dealing with gas samples only), both the WF and the impedance of the conducting polymer are changing. The change of WF can be detected by measuring the ChemFET threshold voltage V_T change (V_T is the minimum potential applied to the gate contact which will allow a current to flow from the drain to source). The change of impedance is detect by applying a small AC signal through the drain and impedance electrodes in ChemFET. Besides these two transduction principles, using different sensing materials in different ChemFETs on a single chip can offer more information about the chemical environment.

1.1.2 Electrochemical tuning of conducting polymer work function

To make good chemical sensor arrays, it is crucial to choose proper materials as the sensing layer. Conducting polymers are good choice for gas analytes in our project. In our design of ChemFET array, on exposure to gas analytes, the change of WF of conducting polymers, which is in linear relationship to the change of V_T, can be accurately detected by the FETs. The modulation follows the equations below,

$$E_F = E_{D^*} + \frac{kT}{2\delta} lnP_G \tag{1.1}$$

$$V_T \propto V_{FB} = \frac{\Phi_{Si} - \Phi_{CP}}{e} \tag{1.2}$$

$$\Delta V_T = \frac{\Delta \Phi_{CP}}{e} \tag{1.3}$$

In the equations above, the E_F, is the fermi level of conducting polymer, E_{D^*} is the fermi level under standard conditions where $P_G = 1$, P_G is the partial pressure of the donor gas, δ is the fraction of transferred charge. V_T is the threshold voltage of FET, V_{FB} is the flat band voltage, Φ_{Si} and Φ_{CP} is the WF of the bulk silicon and conducting polymer sensing layer, e is the electron charge.

Gas molecules and conducting polymers can form charge-transfer-complex (CTC). The ability of this CTC forming depends on the gas molecule's electron "donacity" and conducting polymer's "acceptability". For a specific gas molecule, the conducting polymer matrix can be an electron acceptor or not depending on the work function difference between the gas molecule and conducting polymer. Conducting polymers like Polyaniline, its work function depends on its electronic states, under different doping level, its work function varies. That means, by changing the work function of conducting polymer, we can make it an "acceptor" for a gas molecule. On the other hand, we can also turn the conducting polymer from "acceptor" to "non-acceptor". So, at different electronic state, conducting polymer can have different selectivity to various gas molecules.

The modification of electronics state of conducting polymer can be easily realized by electrochemical methods. It has been well demonstrated that the WF of PANI can be precisely adjusted.[11] To use this principle in our ChemFET sensor array, we need to establish a method of performing electrochemistry inside a single cell on the chip. The challenge here is we have to work on a tiny electrochemical cell, whose dimension is about 500 μm $\times$ 400 μm $\times$ 200 μm. In this chapter, we proposed how to setup a three-electrode system in the

micro-cell, using PPSA as the conducting polymer to demonstrate that it is possible can tune conducting polymer WF with pulse chronoamperometry.

1.1.3 Poly(phenylenesulfidephenyleneamine) (PPSA)

Poly(phenylenesulfidephenyleneamine) (PPSA) is a relatively new polymer that represents the first hybrid structure of polyphenylenesulfde (PPS) and polyaniline (PANI).[12,13] PPSA inherits the favored material properties of both PPS and PANI such as chemical thermal stability, high conductivity and ease of synthesis. This polymer is colorless with a low density. It is soluble in solvents THF, DMF, DMSO NMP and cyclohexanone. The molecular weight is $M_n = 1.5 \times 10^5$ g/mol from size-exclusion chromatography in THF with polystyrene as standard. The polymer is stable up to 380 °C, and has a glass transition temperature (T_g) at 145 °C. The updoped PPSA is completely amorphous and insulating with conductivity lower than 10^{-9} S/cm. PPSA has three different redox states which is show in Fig 1.2. The doping of PPSA can be carried out chemically using conventional oxidants such as bromine, iodine, $SbCl_5$ and $FeCl_3$. The electrochemical methods for precise tuning of PPSA properties has been well studied by Li.[14–16]

In the GT02 design, Chemical sensing layers need to be deposited on the gate area of each ChemFET module, and these areas need to be well separated. This separation is assisted by a permanent epoxy mask on the chip surface. The epoxy mask has eight open cells on the gate areas of the transistors, which ensures the separation among the transistors and also facilitates the individual modification of the sensing layers after they have been deposited. To meet this objective the epoxy mask must satisfy certain requirements:

1. Photo-patternable, which makes it suitable for photolithography in fabrication process

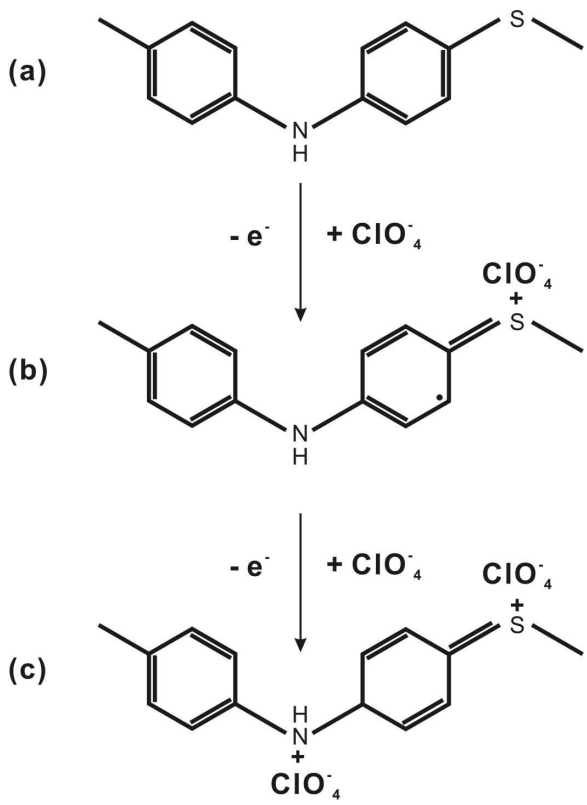


Figure 1.2: The chemical structure of three redox states of PPSA (a) undoped, (b) polaron, (c) bipolaron.

2. Chemical inertness, which ensures the usage of the chip in broad chemical environments.

3. Good adhesion to silicon dioxide, which prevents the leakage and undesirable contact among individual cells.

4. High aspect ratio, which provides greater available volume at the gate area needed for the modification.

5. Similar thermal expansion coefficient to silicon, which prevents the delamination during the wire-bonding when the chip is heated.

1.1.4 Selection of hight aspect ratio materials

High aspect ratio materials are not commonly used in silicon industry, unless special 3-D structure is needed. As a result, there is not many choices for us. Two polymeric materials have been used to make epoxy mask in the past, epoxy SU-8[17,18] from Micro-Chem Corp., and Vacrel® 8130 from Dupont. Even though these two materials have met most requirements, neither of them has been totally suitable for our purpose.

The SU-8 is perhaps the most widely used high aspect ratio material, and it has found many applications in MEMS fabrication and packaging such as the fabrication of plastic micromolds or metal micromolds by electroplating,[19] microfluidics for SU-8 microchannels,[20] fabrication of photoplastic structures such as microgears.[21] It is a negative, UV-sensitive, thick, epoxy-photoplastic resist, yielding high aspect ratio structures, by spin coat in a conventional spinner, it can reach a thickness range from 1 μm to 300 μm, while up to 2mm thickness by multi-layer coatings. In Fig 1.1 and Fig 1.3, the chemical sensor arrays were all covered with SU-8 epoxy mask. Besides its chemical inertness and good initial

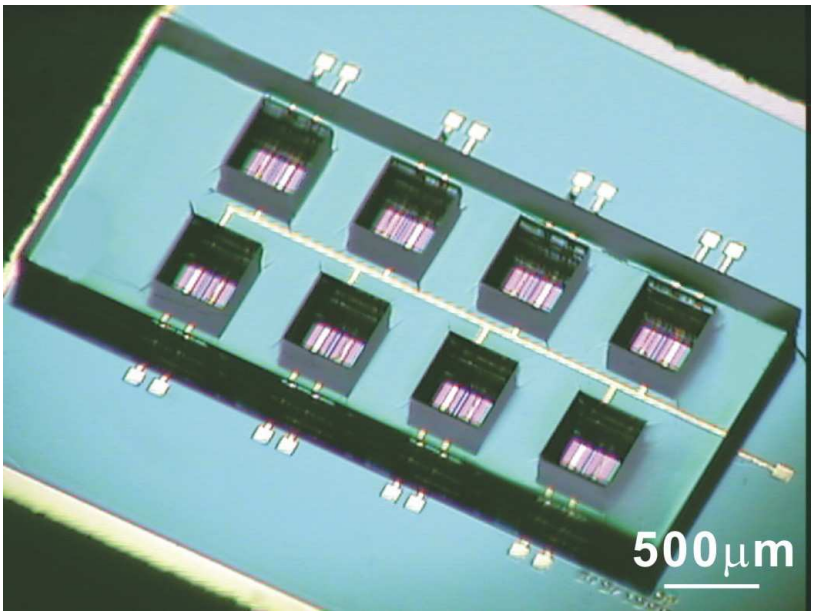


Figure 1.3: GT02 chip covered with SU-8 epoxy mask with the thickness of ~ 200 μm.

adhesion to silicon/silicon dioxide, the main advantage of SU-8 is that it is transparent which makes the alignment step relatively easy. The main drawback of SU-8 is the large difference of its thermal expansion coefficient from that of silicon. Consequently, after a short temperature cycling, e.g. during the wire-bonding step, in which the device chip has to be heated to approximately $100 \sim 120$ °C, the SU-8 epoxy mask cracks and delaminates from the silicon wafer surface. Moreover, even a partial delamination leads to leakage paths between selective layers deposited in the individual wells that prevents their independent modification.

Vacrel® 8130 is a polyimide material that has also been tried. This material is designed for print circuit board protection, it comes in the form of 75 μm thick dry film and is hot-roll laminated onto the print circuit board surface. It has never been used on silicon wafter surface. Tests showed that this material has a good adhesion on silicon/silicon oxide surface, so we used it as high aspect ratio material for building mask. A double layer of Vacrel was

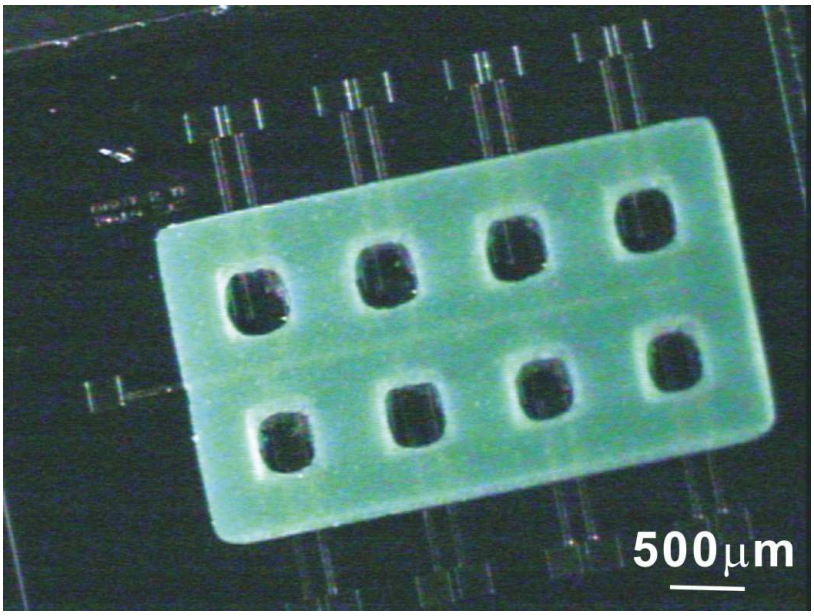


Figure 1.4: GT02 chip covered with Vacrel epoxy mask with the thickness of $\sim$ 150 μm.

hot-roll laminated onto device wafer, and then exposed to UV light and finally developed in a 1% potassium carbonate solution, a thickness of 150 μm has been achieved. Vacrel doesn't have the stress problem as SU-8, it is relatively softer and can resist the thermal cycles. The major problem with Vacrel is due to its dark green color, which makes the alignment difficult. It is completely opaque when 3 layers of 75 μm Vacrel® 8130 films are applied to a wafer. Also because it is isotropic, it is hard to obtain a pattern with sharp edges. The pattern developed by Vacrel is shown in Fig 1.4.

In this chapter, we are discussing another high aspect ratio, spin-on material, PSR-4000BN. It is a commercial product from Taiyo America, Inc. Like Vacrel® 8130, it is also designed for print circuit board protection, and no documentation has been found about the application on silicon industry, but it offers better properties for our application. PSR4000BN is a two-component, alkaline developable, liquid photo-imageable epoxy material, it comes with cross-linker CA40BN. A good quality, high aspect ratio epoxy mask has

been developed using this material. A removal protocol has also been developed.

1.2 Experimental

1.2.1 Mask fabrication process

The epoxy, PSR-4000BN, and the cross-linker, CA- 40BN, both obtained from Taiyo America, Inc. (Carson City, NV) were stored in black boxes in refrigerator and used without any pretreatment. Karl Suss MA-6 Mask Aligner was used for alignment and Hitachi 3500H SEM was used for taking SEM images of the pattern.

PSR-4000BN and CA-40BN were pre-warmed to ambient temperature for over at least 1 hr before usage in cleanroom under yellow light. 10 grams of PSR-4000BN and 4.3 grams of CA-40BN were weighed and thoroughly mixed, and the mixture was then applied to a pre-weighed and cleaned silicon wafer. A two-step spinning procedure was used, 300 rpm at 1000 r/s ramp for 10 sec followed by 1000 rpm at 2000 r/s ramp for 30 sec. After that the wafer was weighed again. The wafer was put on an aluminum top hotplate, baked with a temperature ramp of 2 °C/min until 82 °C, for 2 hr. Pre-baked wafer was then aligned and exposed with a Karl Suss MA6 mask aligner, wavelength used was 405 nm, the exposure energy and time was 13.2 mJ/cm^2 and 55 sec, respectively. The wafer was then developed in warm (∼40 °C) 1% (w/w) potassium carbonate (K_2CO_3) solution for approximately 8 min. A clean paint "spray gun" (Wagner Power Sprayer 1300 psi 1-speed) was used for spray developing. Finally, the wafer was dried with a Semitool Spin Rinse Dryer, and then post-baked at 95 °C for 1 hr.

1.2.2 On-chip micro-cell electrochemistry

GT02 ChemFET sensor array chip was attached to a 28 DIP ceramic header (Edison engineering Inc.) with silver-based conducting epoxy, then wire-bonded to the header with

gold wires. Transistor characteristics were measured with HP 4155A parameter analyzer.

PPSA sample was prepared by Klaus Müllen *et al.* at the Max-Planck-Institute for Polymer Research, Germany.[12,13] During the experiment, PPSA sample was dissolved in cyclohexanone (typical concentration $\sim$ 5 mg/mL), and then cast onto GT02 Chemical sensor array cells with a 10 μL syringe, usually one drop the solution is used for single cast. After casting, the film was vacuum dried for at least 15 min to get rid of the solvent. Fig 1.5 shows the cast PPSA film in ChemFET cell.

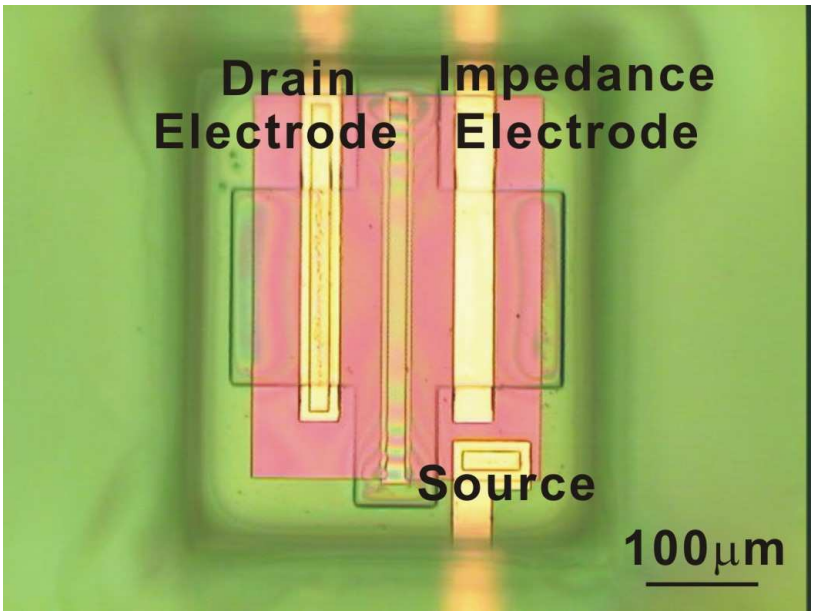
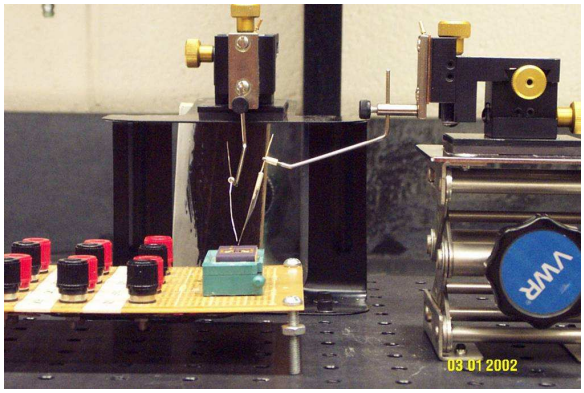


Figure 1.5: GT02 ChemFET with PPSA film cast in the cell, PPSA is transparent in undoped state.

Electrochemical measurements were carried out with EG&G273A potentiostat. The system setup is shown in Fig 1.6. Drain and impedance electrodes of ChemFET were connect together as the working electrode (Fig 1.5), a Pt wire (d=0.25mm)was used as counter electrode, and an Ag wire (d=0.1mm) was used as reference electrode (Ag wired is sealed in a glass capillary and connected to Cu rod with silver-based conducting epoxy). Counter (Fig 1.6(b)) and reference (Fig 1.6(c)) electrode were positioned well inside



(a)

(b)

(c)

Figure 1.6: Three-electrode system for micro-cell electrochemistry, drain and impedance electrodes are connected together as working electrode, and are connected to potentiostat through lab made circuit board, Pt counter electrode and Ag wire reference electrode are positioned into ChemFET cell with Micro-positioners. (a) Whole setup for electrochemistry (b) Pt counter electrode, d=0.25mm (c) Ag reference electrode, d=0.1mm.

the ChemFET epoxy cell through two micro-positioners (Quater Research & Development Inc. XYZ-300-TR). All the measurements were carried out in 0.1 M $LiClO_4$/Propylene Carbonate (PC) solution.

1.3 Evaluation of epoxy mask quality

1.3.1 Determination of mask aspect ratio

High aspect ratio is one of the most important properties when we search for proper material for chemical sensing application. Aspect ratio is defined as the length of the vertical axis divided by the length of the horizontal axis. In practical terms a high aspect ratio means that we can build deep wells on the chip, and larger amount of electrolyte or other modifying solutions can be held in the wells during the post-treatment step. The SU-8s ability to produce high aspect ratio patterns in photolithography has been demonstrated in recent years,[18,22–25] aspect ratio as high as 50:1 has been achieved by this material. Aspect ratios from 8:1 to 16:1 have been achieved by us with Vacrel and PSR-4000BN. Fig 1.7 shows the comparison among 3 different epoxy masks, SU-8 mask has the best quality, the PSR4000BN mask is almost as good as SU-8 mask, while the Vacrel mask shows the poor aspect ratio. An SEM image of PSR-4000BN epoxy mask is shown in Fig 1.8. The estimate of the aspect ratio of the material from a SEM image is shown in Fig 1.9. On the SEM image of the mask profile, the aspect ratio can be obtained from the ratio of thickness to the extension on X axis. For example, from Fig 1.9, an aspect ratio of 11:1 can be estimated. The accuracy of this estimation is always influenced by the fabrication process such as: thickness of the spin-on material, the exposure time and the development. With PSR-4000BN/CA40-BN, epoxy masks as thick as 166 μm have been successfully made. Development of thicker films presents difficulties. It is hard to pre-bake the epoxy well and

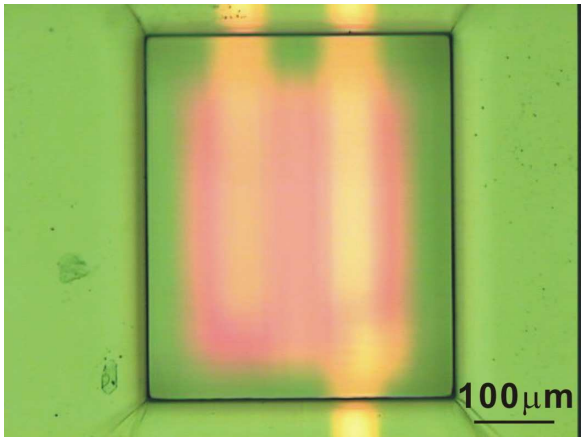
to completely remove the residues left in the wells after the development step.

1.3.2 Test of chemical resistance

Sensing layer modification always involves solvent contacts such as dipping chips into solution or casting solution into wells of the mask. This means that the mask must be stable in most common solvents. The stability tests were performed and the results are shown in Table 1.1. From the 72 hour test results shown in Table 1.1, we can see that PSR-4000BN is stable in most solvents that are widely used for casting selective layers in chemical sensors and in the electrochemical modification process. Formic acid is somewhat an exception because several hour-long exposure softens the fully developed epoxy mask. Formic acid is one of the best solvents for spin-casting polyaniline layers.[26] After depositing PANI/formic acid solution into the wells, the PANI film is usually re-doped with other acid dopants. The exposure to formic acid usually takes only a short time, in which the deleterious effect on the epoxy mask is negligible. However, a long time contact with formic acid should be avoided.

1.3.3 Test of mechanical quality

Mechanical properties such as adhesion and hardness are also important. Good adhesion to silicon nitride/dioxide surface and sufficient hardness for maintaining the shape are required. A simple indentation test with a dental probe was made on each material. Qualitative results of these three different thick materials are given in Table 1.2. An attempt to mechanically remove patterned epoxy mask always resulted in its fracture but not in the separation from the wafer.



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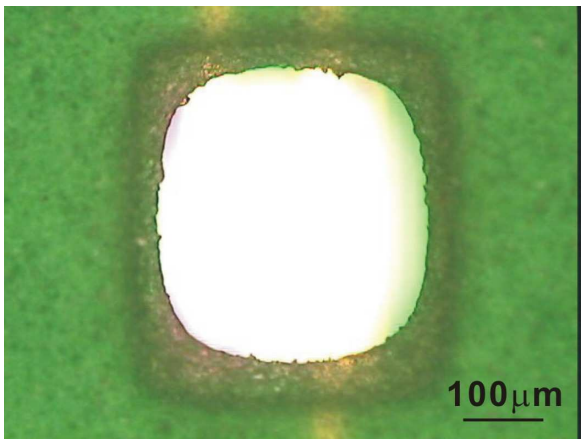

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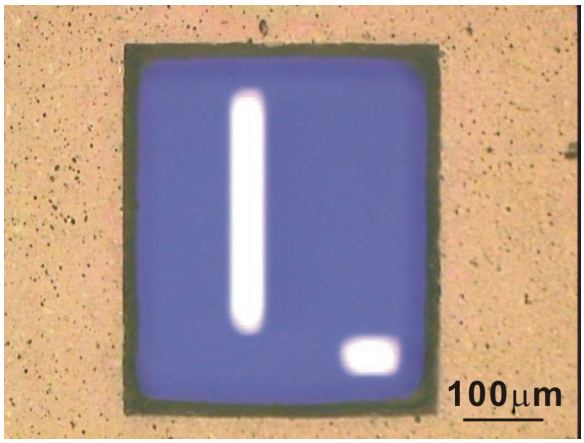


(c)

Figure 1.7: Comparison between different epoxy masks: (a) SU-8 epoxy mask with a thickness of 200 μm, (b) Vacrel epoxy mask with a thickness of 150 μm and (c) PSR4000BN epoxy mask with a thickness of 166 μm.

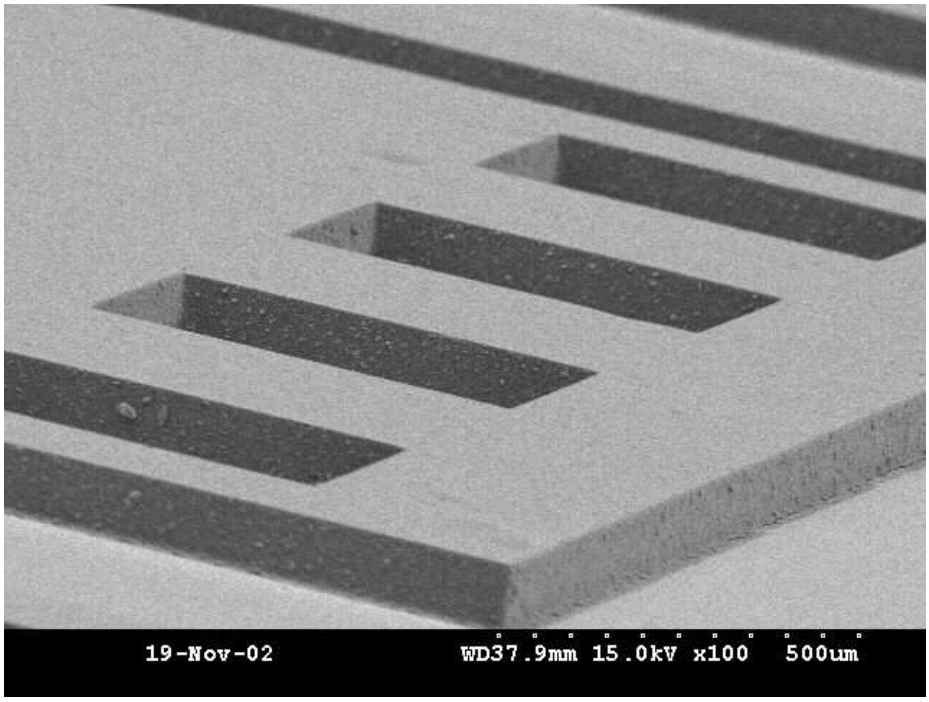


Figure 1.8: SEM image of the 80 μm thick PSR4000-BN epoxy mask.

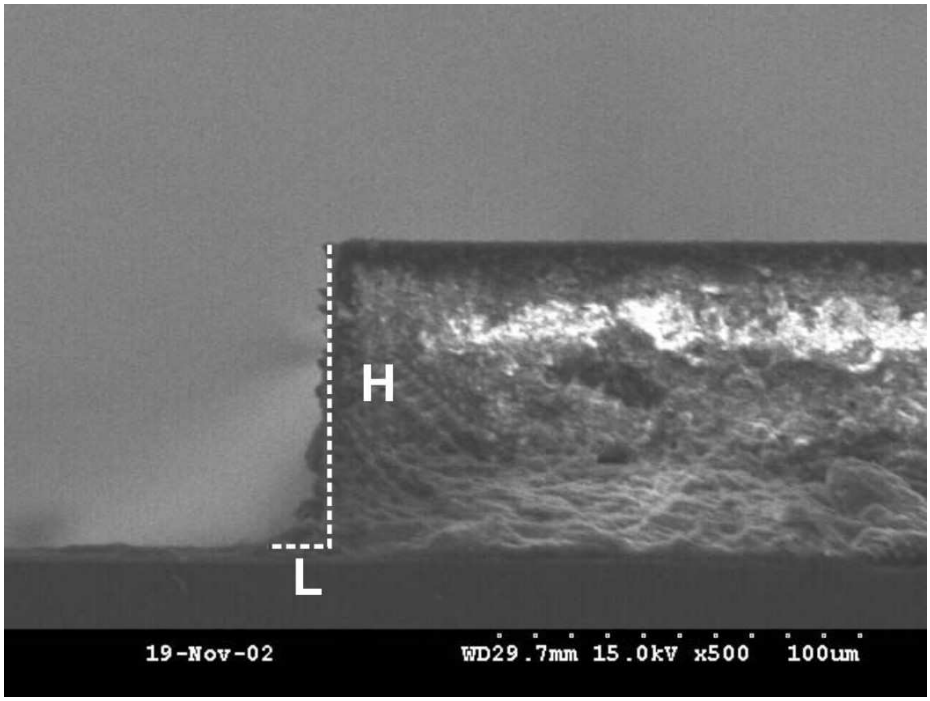


Figure 1.9: Estimate of aspect ratio from SEM image. Aspect Ratio=H/L.

Table 1.1: Stability of fully cured PSR-4000BN epoxy mask in different solvents

Type of Solvent	Provider	Observation
DI water	Lab prepared	No change
Propylene Carbonate	Sigma-Aldrich, 99.7% HPLC grade	No change
Formic Acid 88% in water	J.T.Baker, A.C.S. Reagent	Pealed from surface after 24 hour, dissolved slowly
Acetone	Fisher Scienific, Certified, A.C.S. Reagent	No change
Acetonitrile	Aldrich, 99.93+% HPLC grade	No change
HCl (1M) aqueous	J.T.Baker, A.C.S. Reagent	No change
H_2SO_4 (1M) aqueous	J.T.Baker, A.C.S. Reagent	No change
DMF	Fisher Scientific, Certified, A.C.S. Reagent	No change
Methanol	Fisher Scientific, Certified, A.C.S. Reagent	No change

Table 1.2: Qualitative comparison of mechanical properties among three different materials

	SU-8	Vacrel	PSR-4000BN
Status	Very hard	Softer	Hard
Indentation	Break Before Peal	Break before peal	Break before peal

1.3.4 Stripping epoxy mask

Stripping off a cured epoxy is an important process in IC fabrication and MEMS applications. The stripping process allows to "rescue" the wafer if necessary. Various approaches such as oxygen plasma ashing or laser ablation are normally used for stripping off SU-8. We found that PSR-4000BN can be conveniently stripped off by dry or wet process. This is a major advantage over other thick mask materials. The etch rate in dry oxygen plasma was approximately 3 μm/min . After approximately 3 min, the epoxy begins to crack, and after 4 min, the epoxy becomes so loose that it can be easily removed by nitrogen blast or by swabs. The epoxy can be removed also by wet etching in 10 min in 1% aqueous potassium carbonate (K_2CO_3) solution at 100 °C. The white residuum from the inorganic filler can be removed by further treatment in the 1% K_2CO_3 solution at 80 °C for 90 min. Wafer stripped with wet etch is generally cleaner than that stripped by dry plasma etching.

1.4 Electrochemical tuning of PPSA work function

Electrochemical doping of PPSA has been systematically studied by Guofeng Li.[14–16] Usually in those studies, PPSA film was cast on a Pt foil or a disk electrode surface, and the electrolyte is $LiClO_4$ in acetonitrile. Acetonitrile is used not only because it is a good solvent for $LiClO_4$, but also because it can swell the PPSA film well which makes the ions in solution easily enter the PPSA film matrix. In this project, acetonitrile has a big disadvantage - the low boiling point which makes it very volatile. Because of the volume in the cell is so small ($\sim 4 \times 10^{-8}$ L), acetonitrile would evaporates just in few min. Propylene carbonate (PC) is used as the substitute of acetonitrile in this study. PC has a boiling point of 240 °C, and shows good solubility of $LiClO_4$, it also swells PPSA film well. So in this

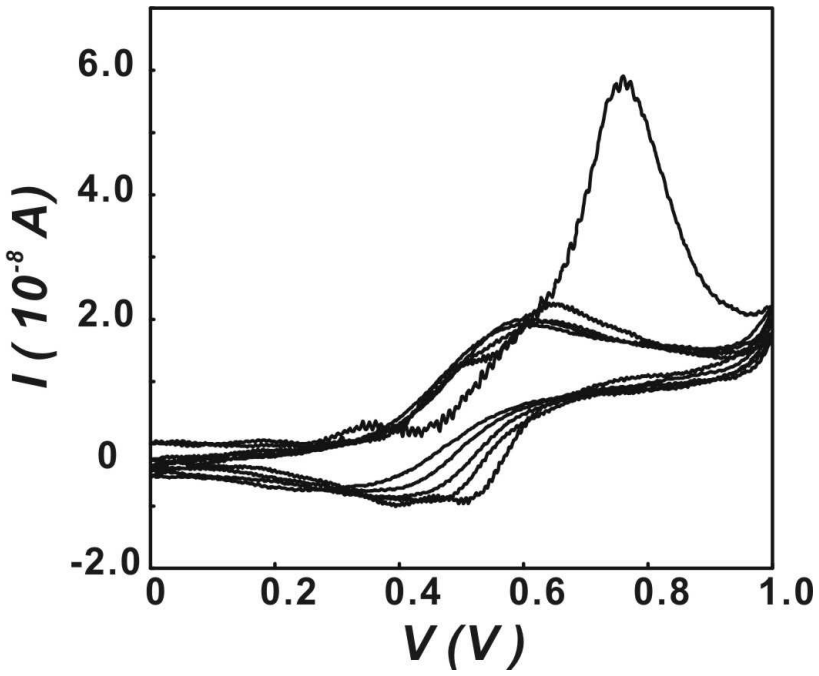
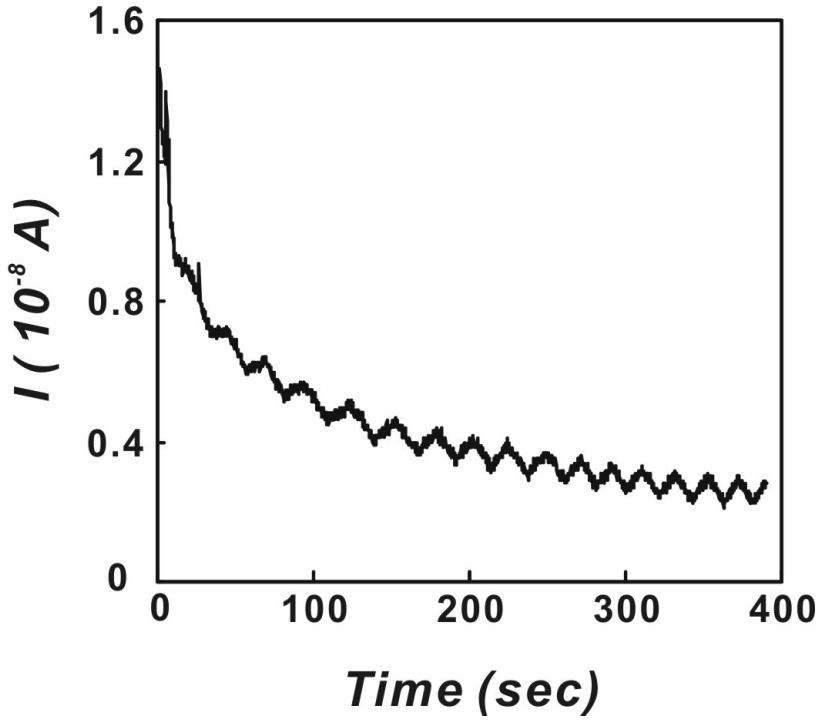


Figure 1.10: Cyclic voltammogram of PPSA film in single ChemFET cell on chip in 0.1M $LiClO_4$/PC solution, scan rate = 50 mV/sec, V vs Ag/Ag^+.

in-cell electrochemistry, 0.1 M $LiClO_4$/PC solution is used as the electrolyte.

Fig 1.10 is a typical cyclic voltammogram of PPSA film in ChemFET cell. In general, the polymer is oxidized during the positive scan. The oxidation of PPSA is accompanied by the influx of the ClO_4^{-1} ions in to the film to maintain the overall charge neutrality. In the reverse scan, the PPSA film is reduced and the ClO_4^{-1} ions is expelled from the matrix into the solution. The sharp peak at first cycle appears at more positive position because the tight packing of the polymer chain hinders the ClO_4^{-1} ions from entering the film matrix. The spectrum study[15] shows that PPSA has three redox states shown in Fig 1.2. Under microscope, the doped PPSA film shows a dark color while the undoped PPSA is almost transparent. From this, we can easily tell the level and the distribution of ClO_4^{-1} doping in PPSA film.

The change of PPSA work function is closely associated with the redox state of PPSA.



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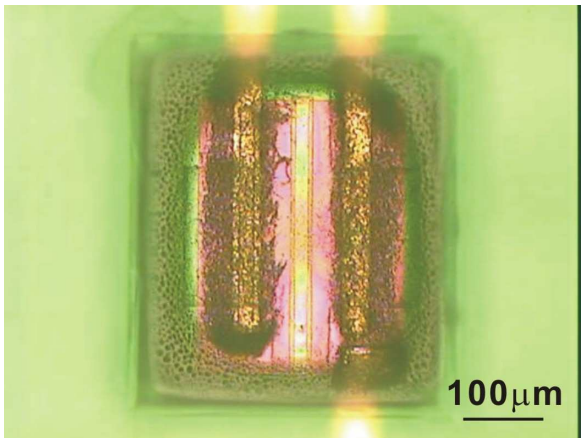


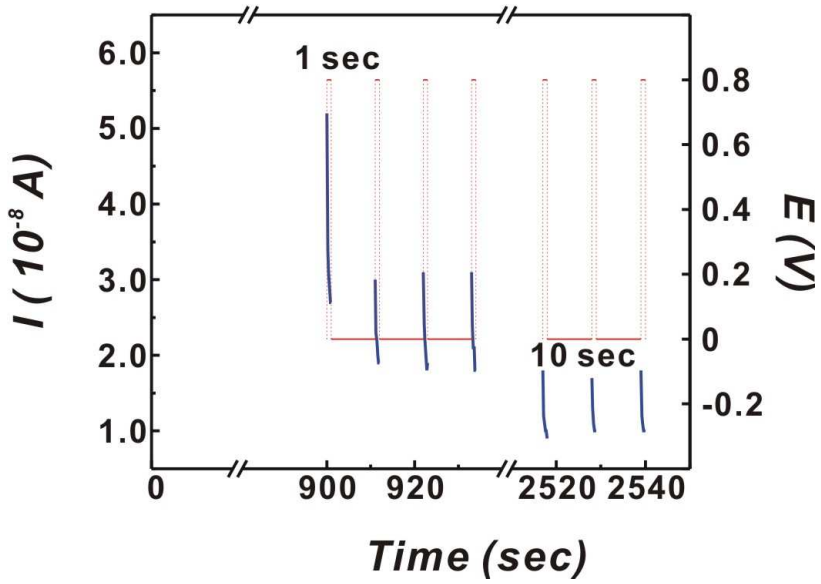
(b)

Figure 1.11: Chronoamperometry of PPSA doping in single ChemFET cell, V= 0.8V, V vs Ag/Ag^{+}. (a) I∼t characteristic of chronoamperometry of PPSA, (b) photograph of doped PPSA in ChemFET cell.

The redox state of PPSA is controlled by doping potential. So tuning of PPSA work function can be realized by performing chronoamperometry on PPSA film. Fig 1.11 shows the chronoamperometry of PPSA doped at 0.8V. From the photograph we can see that only the PPSA in the vicinity area of electrodes is doped, in the center where the gate of ChemFET locates, the PPSA remains undoped or very lightly doped. The reason is that the undoped PPSA film is very compact and resistive, most ClO_4^{-1} ions can just enter the electrode vicinity area, they can't travel to the center gate area.

In order to dope the PPSA in the gate area well, first, we need to make the PPSA film less dense, so ClO_4^{-1} ions can easily penetrate, second, we need to let ClO_4^{-1} ions travel along the PPSA film to the center gate area. To make the film less dense, we can let the film soak and swell in PC electrolyte for longer time. To make the ions travel inside the PPSA film, pulse chronoamperometry is a good choice. In pulse chronoamperometry, we first give a short voltage pulse then followed by a delay period which no voltage is applied, this forms a cycle, by repeating the cycles, we can gradually move the incorporated ions to the center area and change the PPSA work function there. In Fig 1.12 shows a typical pulse chronoamperometry voltammogram, in one cycle, a 1 sec 0.8V pulse is followed by 10 sec delay time. After 150 cycles, we can see clearly the the center gate area is well doped.

Using pulse chronoamperometry, we can control the doping level of PPSA film, thus tune the work function of PPSA film. By doping PPSA film at different doping potential, we can have a series of PPSA film with different work function. From equation 1.3, we know the relative change of V_T is in linear relationship with relative change of WF. In Fig 1.13, we can clearly see how work function is precisely tuned by changing the doping potential. Fig 1.13 shows that V_T tends to increase when the doping potential increases. But the result is not very satisfactory because the difficulty in the V_T measurements. In all the



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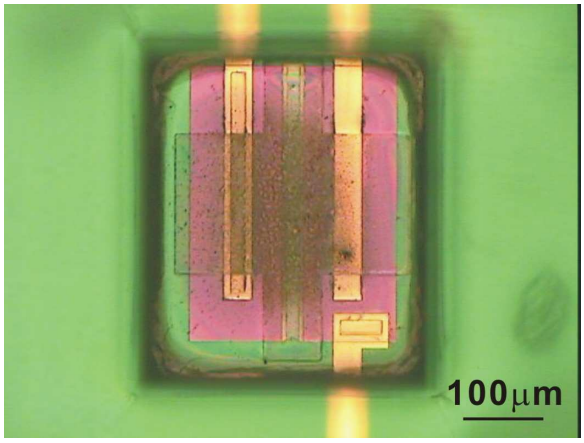


(b)

Figure 1.12: Pulse chronoamperometry of PPSA doping in single ChemFET cell, V= 0.8V, V vs Ag/Ag^+. (a) I∼t and V∼t curve of pulse chronoamperometry of PPSA, red line is the voltage pulse applied, blue line is the current collected on the working electrodes, (b) photograph of doped PPSA in ChemFET cell after 150 cycles.

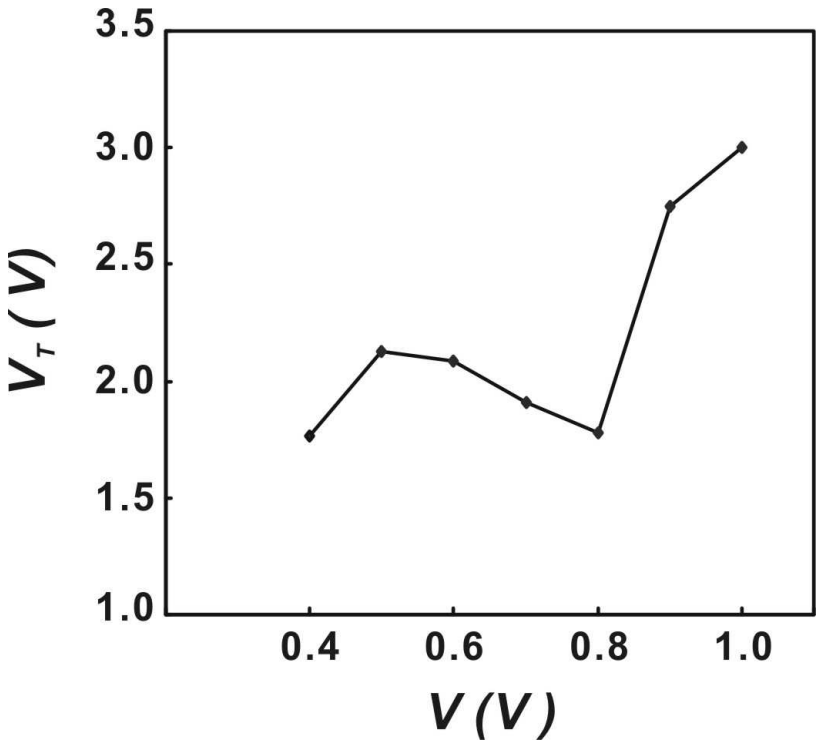


Figure 1.13: ChemFET threshold voltage V_T as function of the doping potential of PPSA in cell, V vs Ag/Ag^+.

measurements, same PPSA film was used. After each doping process, electrolyte has to be removed and ChemFET has to be cleaned with solvents such as H_2O or methanol (solvents like acetone acetonitrile should be avoid because they can easily take the doped ions away from the film, then dedoped the film), and then dry in vacuum to remove the influence from solvents. During this process, it is hard to control the loss of ClO_4^{-1} ions. Also the level of swelling of the PPSA film can affect the V_T measurement which is difficult to characterize. Improved methods have to be developed to solve this problem.

1.5 Conclusions

It has been demonstrated that PSR-4000BN is an excellent material for fabricating permanent thick epoxy masks with high aspect ratio and a sharp side profile. Good mechanical properties combined with excellent chemical resistance to common chemical solvents ensure

its application in various sensing preparations in which liquid environments are encountered. The cured mask can be easily stripped off. Therefore it is a material of choice for fabrication of chemical sensor array.

Electrochemical tuning of work function of conducting polymer in micro-cell on chip can be realized with a three-electrode system. Propylene carbonate is good solvent for making electrolyte in this in-cell electrochemistry for it low evaporation rate and ability to swell the PPSA film. Using pulse chronoamperometry, the PPSA film in the ChemFET gate area has been doped successfully. A general trend between ChemFET threshold voltage and PPSA doping potential has been evolved.

CHAPTER II

CHEMICAL EFFECTS ON ORGANIC ELECTRONICS

2.1 Introduction

Organic electronics as the complement of conventional silicon and gallium arsenide semiconductors based inorganic electronics have become more and more important in recent years. Organic electronics includes organic field-effect transistor (OFET), organic light emitting diode (OLED),[27] organic photovoltaic devices etc. Most organic electronics are based on organic semiconductors, which offer advantages due to their unique mechanical properties as well as their compatibility with the low-cost fabrication techniques. Intensive research has been made on improving the materials properties. Despite their promising future, some fundamental problems with organic electronics remain to be solved. In this chapter, we discuss influence of chemicals present in the ambient environment on the properties of organic electronics.

2.1.1 Influence of ambient environment on organic electronics

From early stage, people recognize the fact that the ambient environment can and does affect organic electronics and this subject has been recently reviewed.[28–30] By "ambient" we mean chemical species in the gaseous atmosphere that surround the device, in which the organic semiconductor (OS) plays a major functional role. The chemical species include both the majority components present in clean air, namely, oxygen, nitrogen, and water vapor, as well as minority components, such as hydrogen, hydrogen sulfide, ammonia, amines, etc. These chemical species can have variable interactions with organic electronics which

can be either reversible or irreversible. In contrast, conventional silicon-based electronics is virtually immune to the environmental interferences because silicon dioxide and silicon (oxy)nitride are almost ideal passivation for most solid-state devices operated under normal conditions. If needed, further protection is provided by additional encapsulation.

Chemical effects can be utilized in many applications. For example, the effect of gaseous species on OS is beneficial in solid-state chemical sensors for gases that utilize those materials. In such case, the changes of electronic and optical properties of the OS or the controlled effects on the device structure are the basis of robust and well functioning transduction principles. In other words, in chemical sensors the OS becomes a vehicle by which the chemical interaction is transformed into defined electrical or optical signals. There is extensive literature covering this subject.[31–38] On the other hand, such interactions could be viewed as detrimental in electronics intended for signal and information processing or for optoelectronics.

In this chapter we take a closer look at the origin and effects that chemical environment can have on organic electronics. We shall consider chemically induced changes in the bulk electronic properties of the OS, namely, the changes of work function (WF) and conductivity, chemically induced changes of the barriers at the OS/metal junctions, and the effect of sorbed species on the interface between the OS and the dielectric substrate that is used as its support.

2.1.2 Equivalent circuit of general organic electronics

Practically, any device or a test structure involving the OS can be represented by the equivalent impedance network shown in Fig 2.1. Chemical effects play separate but specific roles at the individual elements of that circuit, yet measurement of the transfer function

at points A and B yields only the overall relationship between applied voltage and the resulting current. It is therefore important to consider the individual impedances separately, because an incorrect assignment of their origin may lead to an incorrect interpretation of the properties of the OS and/or of the function of the device. The measurements are done usually in the DC mode; however, including capacitors and presenting the individual circuit elements as impedances, as in Fig 2.1, has its advantages if the device is investigated by some AC impedance technique. In this chapter we examine separately chemical effects on bulk, contacts, and interface.

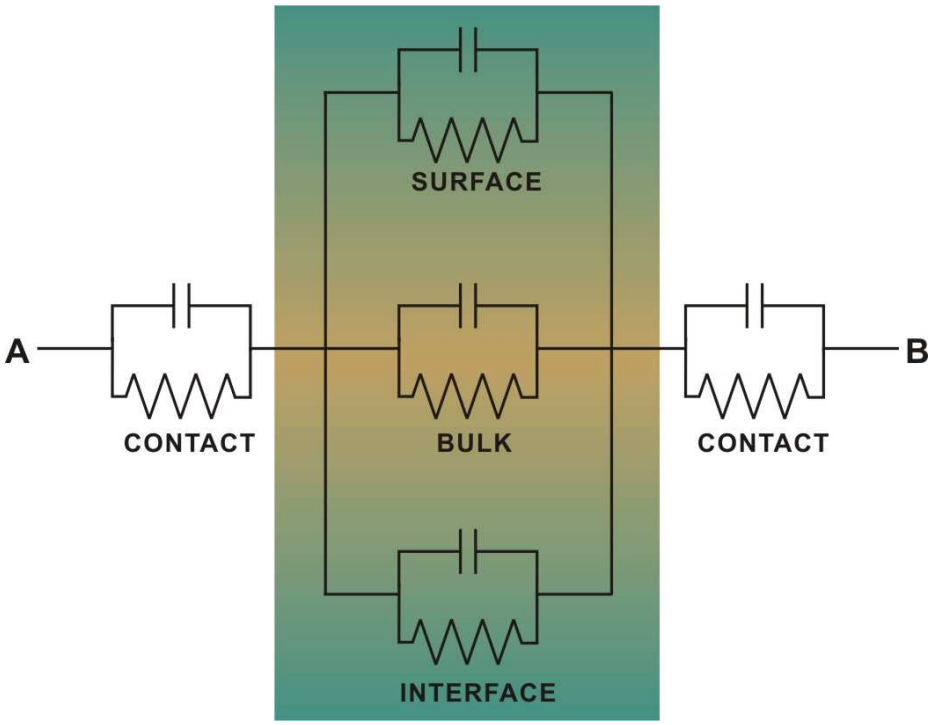


Figure 2.1: Equivalent circuit diagram of general organic electronic device. The surface, bulk, and interface impedances belong to the organic semiconductor (OS). Contacts represent interface between the metal and the OS.

2.1.3 Test platform GT03

To elucidate the chemical effects and compare the performance and function of the OS in an "Organic Field-Effect Transistor" (OFET) with that of a silicon-based "insulated

gate field-effect transistor" (IGFET), the test platform shown schematically in Fig 2.2, has been designed and fabricated. It has all the features of conventional silicon IGFET except that it has two gate contacts over which the layer of OS gate is deposited. A two-layer gate dielectric is formed by 80 nm of thermally grown SiO_2 and 80 nm of chemically vapor deposited, high-temperature silicon nitride. The gate dielectric has sufficient thickness and quality to ensure that there is no parasitic gate leakage current even when unusually high gate voltages (i.e., >20 V) are applied across it. It has been tested in our laboratory with two OS: polyaniline (PANI) and poly(phenylenesulfidephenyleneamine) (PPSA).[12,15] The contacts between clean Au electrodes and either of these two OS are ohmic, as confirmed by examination of the shape of the I-V curves.

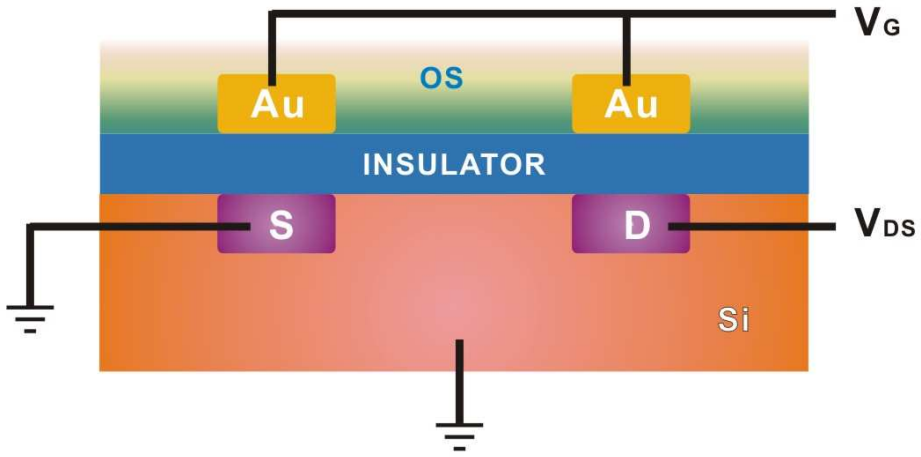
The test platform can be operated as a regular IGFET as shown in Fig 2.2(a), a common gate-to-source voltage, V_G, is applied to both contacts and drain-to-source current, I_D, flows in silicon, between n-doped drain and source electrodes. It follows the normal equations valid for IGFET.[39] For $V_D < V_G - V_T$, in the so-called subthreshold (or linear) region, the current is linearly dependent on the applied drain-to-source voltage V_D

$$I_D = \frac{\mu C_0 W}{L}(V_G - V_T - \frac{V_D}{2})V_D \tag{2.1}$$

In the saturation region, $V_D > V_G - V_T$, I_D is independent of V_D but is quadratically dependent on V_G - V_T

$$I_D = \frac{\mu C_0 W}{2L}(V_G - V_T)^2 \tag{2.2}$$

The other parameters in equation 2.1,2.2 are mobility of minority carriers, μ, gate capacitance, C_0, and the geometrical factors of the device, i.e., the width (W) and the length



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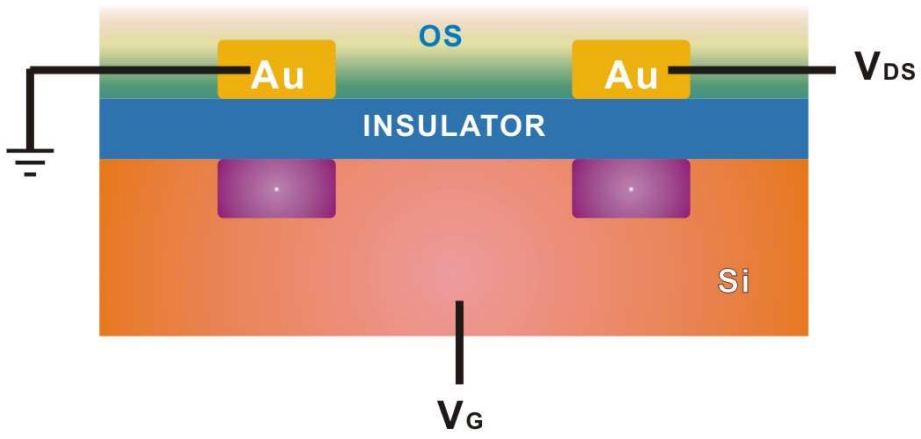


(b)

Figure 2.2: Schematic diagrams of the test platform GT03 that can be operated as (a) insulated gate field-effect transistor (IGFET) and (b) organic field-effect transistor (OFET).

(L) of the channel. The threshold voltage, V_T, is sometimes called the "turn-on voltage" that separates the operation of IGFET in the "ON" and "OFF" state. It is important in defining the "ON/OFF" ratio, which is often used as the figure of merit in the description of OFET. Threshold voltage is also important in ChemFETs because the chemical modulation of the WF of the OS causes the shift of V_T.[37,40,41] Equations 2.1, 2.2 describe the well-known transistor characteristics of classical Si-based IGFET. It is therefore not surprising that any deviation from the shape of these ideal characteristics is the first indication of a potential problem in devices that depend on analogous semiconductor field-effect in OS.

This platform can be operated also as an OFET when it is connected as shown in Fig 2.2(b). In this case the two Au contacts are designated as "drain" and "source", respectively, and V_G is applied to the p-Si substrate. The drain-to-source current then flows through the organic semiconductor, and the field modulation takes place in the OS, somewhere in the gate region above the gate dielectric. In most cases, OFET also follows the equations listed above, but with several assumptions that the organic semiconductors has a constant charge mobility, equal free carriers and dopant density.[42] Here we want to mention again, if the postulated function of the OS is similar or equivalent to the Si, then the output characteristics of OFET should have a similar shape to those obtained with Si-based IGFET of the same geometry. In other words, this platform is a simple diagnostic tool.

2.1.4 Fundamentals of semiconductor/metal contact

Metal-semiconductor contact is a very important component of any semiconductor device. Unlike connected metals, the semiconductor/metal contact is assumed to have higher resistance. In particular, a large mismatch between the Fermi energy of metal and

semiconductor can results in a high-resistance rectifying contact. In organic electronics, organic semiconductor/metal contact plays a crucial role in its functionality. It is important to have deep look into the basics of the interfacial properties.

Fig 2.3 shows the energy-band diagram when organic semiconductor is in intimate contact with metal. In the figure, ϕ_M is the work function of metal, χ is the electron affinity of the semiconductor, ϕ_{Bn} is the barrier height, E_C, E_V are the conduction band and valance band of the semiconductor and E_F is the fermi energy level and q is the unit charge. The potential barrier ϕ_{Bn} formed between the metal and semiconductor prevents most charge carriers (electron or holes) from passing from on to the other. Only those carriers with enough energy can get over the barrier and cross to the other material. Depending on the barrier height, the semiconductor/metal contact could be either ohmic contact or barrier contact.

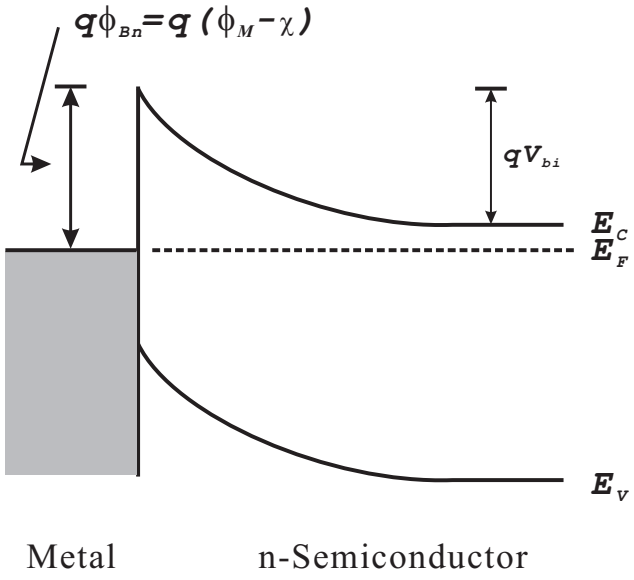


Figure 2.3: Energy-band diagram of metal/semiconductor contacts.

Ohmic contact exits where the barrier height is very low, or the barrier is very narrow, in the latter situation, the carriers (electrons or holes) can actually "tunnel"through the barrier that they don't have enough energy to pass over (Fig 2.4).

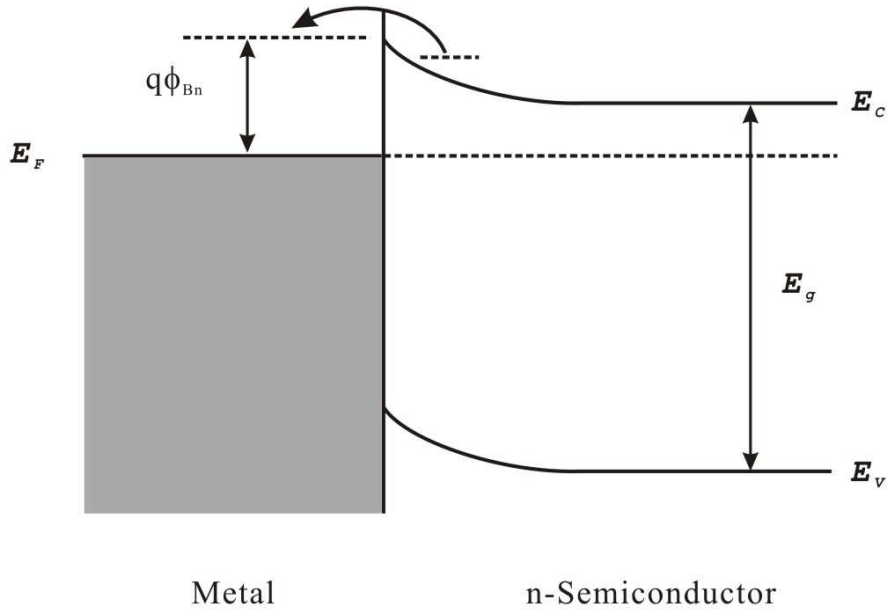
In the ohmic contact, the current voltage relationship follows the Ohm's Law, Equation(2.3). In this equation, J is the current density, e is the charge of an electron, N_0 is the number of free electron per unit volume, μ is their mobility, V is applied voltage, and L is the sample length.

$$J_{OHM} = eN_0\mu\frac{V}{L} \tag{2.3}$$

At low voltage, the current is determined by the motion of the free electrons that are present in the semiconductor. When the voltage increases, electrons injected from the contact outnumber the electrons that are initially present inside the semiconductor. Then it enters the space-charge-limited (SCL) regime, where the current voltage relationship follows the Mott-Gurney Law, Equation 2.4. In this equation, ϵ_i is the insulator dynamic permittivity. The equations 2.3 and 2.4 describe the *bulk-limited current*, it is either ohmic or space-charge-limited.

$$J_{SCL} = (\frac{9}{8})\epsilon_i\mu\frac{V^2}{L^3} \tag{2.4}$$

When a bias is applied to the semiconductor/metal junction, it can either lower the barrier height from the semiconductor side or make it higher (Fig 2.5), but the bias does not change the barrier height from the metal side. In this figure, $q\phi_{BO}$ is the intrinsic barrier height , $q\phi_{Bn}$ is the barrier height at thermal equilibrium, $\Delta\phi_F$ and $\Delta\phi_R$ are the barrier lowering s under forward and reverse bias respectively. The result is a Schottky Barrier



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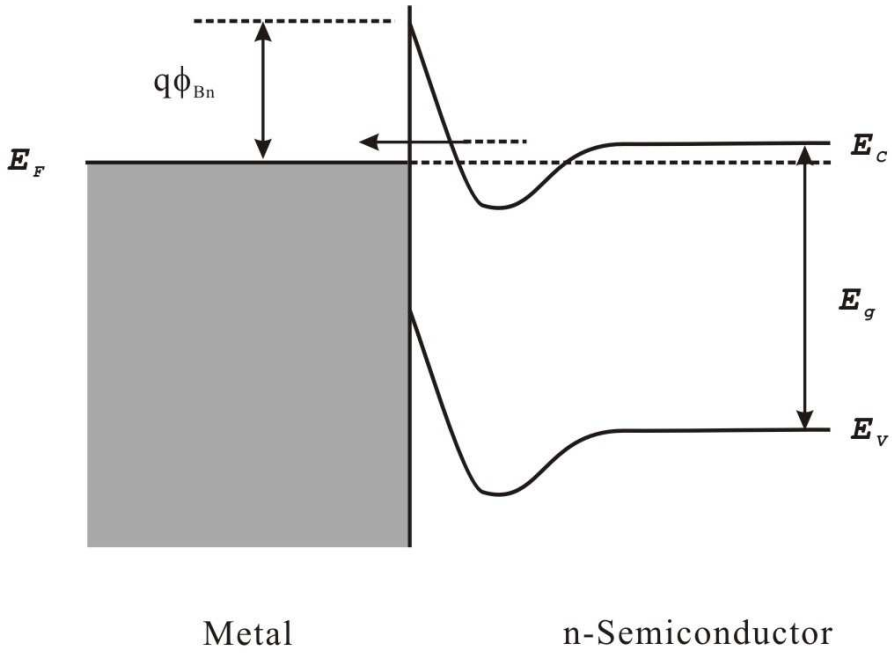


(b)

Figure 2.4: Energy-band diagram for Ohmic contact (a) low barrier height (b) "tunnelling" under high doping.

Table 2.1: Basic conduction processes in insulators[39]

Processes	Expression	V and T Dependance
Schottky Emission	$J = A^*T^2exp[\frac{-q(\phi_B-\sqrt{q\mathcal{E}/4\pi\epsilon_i})}{kT}]$	$\sim T^2exp(+a\sqrt{V}/T - q\phi_B/kT)$
Frenkel-Poole Emission	$J \sim \mathcal{E}exp\Big[\frac{-q(\phi_B-\sqrt{q\mathcal{E}/\pi\epsilon_i})}{kT}\Big]$	$\sim Vexp(+2a\sqrt{V}/T - q\phi_B/kT$
Fowler-Nordheim Emission	$J \sim \mathcal{E}^2exp\Big[-\frac{4\sqrt{2m^*}(q\phi_B)^{3/2}}{3q\hbar\mathcal{E}}\Big]$	$\sim V^2exp(-b/V)$
Space-Charge-Limited	$J = \frac{9\epsilon_i\mu V^2}{8d^3}$	$\sim V^2$
Ohmic	$J \sim \mathcal{E}exp(-\Delta E_{ae}/kT)$	$\sim Vexp(-c/T)$

(rectifying contact), where the junction conducts for one bias polarity, but not the other. Schottky contacts can be used for making good diodes, and can even be used to make a kind of transistor, but for most of application in organic electronics, they are not desired features. Schottky contact is not the only type of barrier contact. Under high electric field ,charge carrier injection in dielectric have two different models: Fowler-Nordheim (FN) model for tunnelling injection and the Richardson Schottky (RS) model for thermionic emission. The FN model ignores image charge effects and invokes tunnelling of electrons from the metal through a triangular barrier into unbound continuum states. The basic conduction process in semiconductors are listed in Table 2.1

In Table 2.1, A^* is the effective Richardson constant, ϕ_B is the barrier height, $\mathcal{E}$ is the electric field, ϵ_i is the insulator dynamic permittivity, m^* is the effective mass, d is the insulator thickness, ΔE_{ae} is the activation energy of electrons, ΔE_{ai} is the activation energy of ions, $a \equiv \sqrt{q/(4\pi\varepsilon_i d)}$, and $V = \mathcal{E}d$, positive constant independent of V or T are b, c and d'.

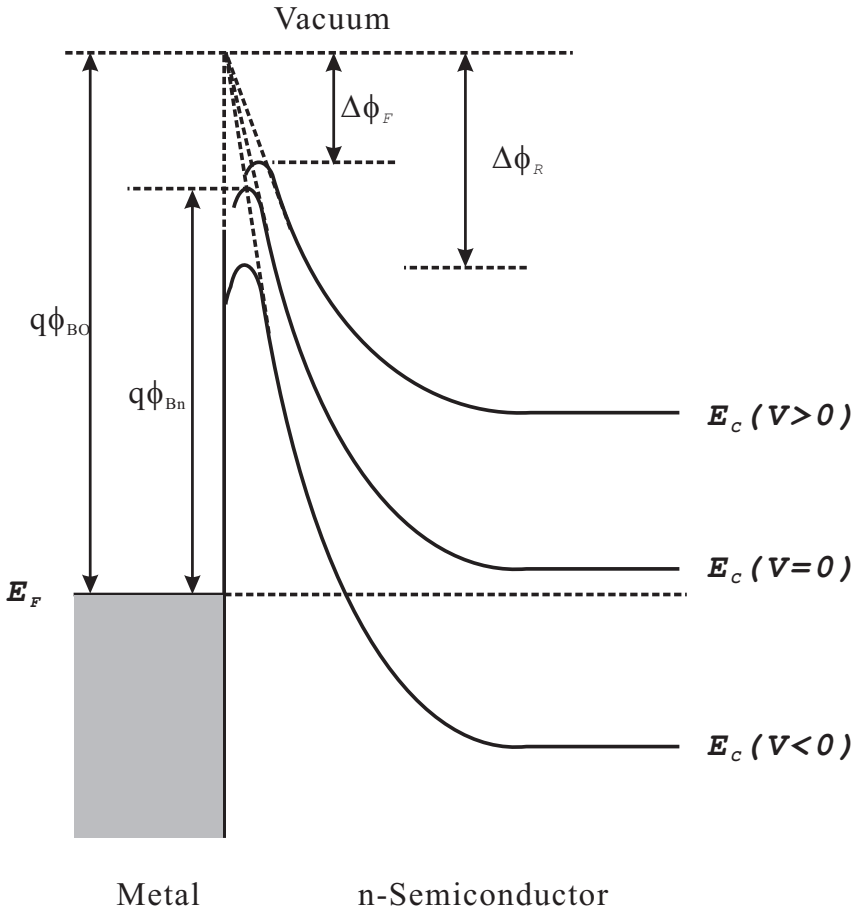


Figure 2.5: Energy-band diagram of metal/semiconductor contacts incorporating Schottky effect for a metal n-type semiconductor under different biasing conditions.

Organic semiconductors are mostly p-type π-conjugated materials which have fairly high work functions. To match the high work function of the material, usually Au is used in organic electronics. Ambient environment can have various influence on the contacts which are often overlooked in the researches. In this chapter, the modulation of contact is discussed in detail.

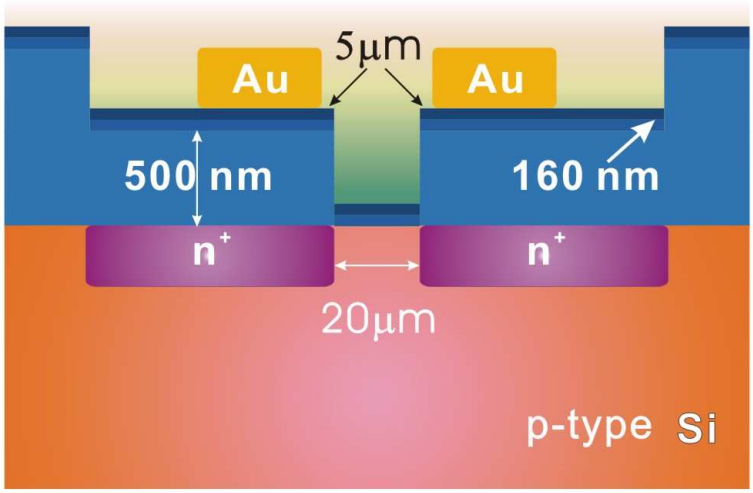
2.2 Experimental

2.2.1 Fabrication of the platform GT03

The fabrication of GT03 IGFET/OFET platform follows a standard n-MOS process with only minor changes. This test platform is an array with eight identical modules on a single chip. First major difference from standard n-MOS fabrication comes from the use of conducting polymer as the gate material. So here we use a noble metal (Au) as the contact, because Au is very chemically inert and has a high work function which matches the work function of π-conjugated organic semiconductor materials. Au electrodes are deposited on top of 500 nm thick field oxide (SiO_2) which is deposited by CVD method. Second, we use a double layer dielectric as the gate insulator. The double layer is consisted of 80 nm of silicon oxide (SiO_2) and 80 nm of silicon nitride (Si_3N_4) as shown in Fig 2.6(a). The nitride layer reduces the possibility of pinhole defects and ensures good passivation. It is deposited by a high temperature, low-pressure chemical vapor deposition (LPCVD) process.

Third change is that a 150-μm-deep epoxy masks are built around each transistor module as shown in Fig 2.7(a) as described in chapter I. In Fig 2.7(b), the "cross" inside each well is the outline of the SiO_2 mask deposited over the Au contacts. It defines the contact area between the Au and the organic semiconductor.

There is a 1000-nm-thick SiO_2 mask deposited over the gold contacts. Its purpose is



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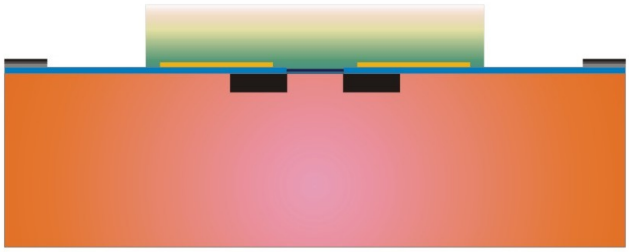
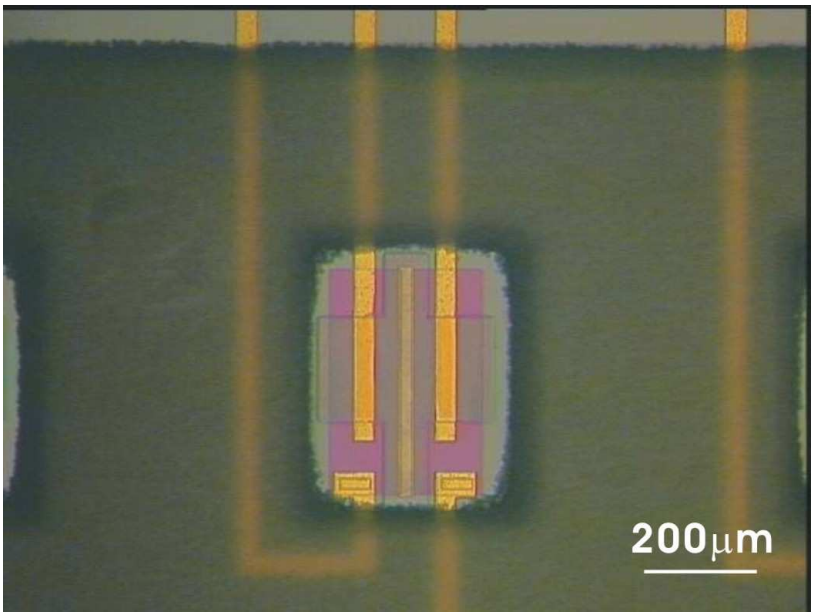


(b)

Figure 2.6: Schematics of cross-section of GT03 test platform (a) schematic not to scale (b) schematic to scale.



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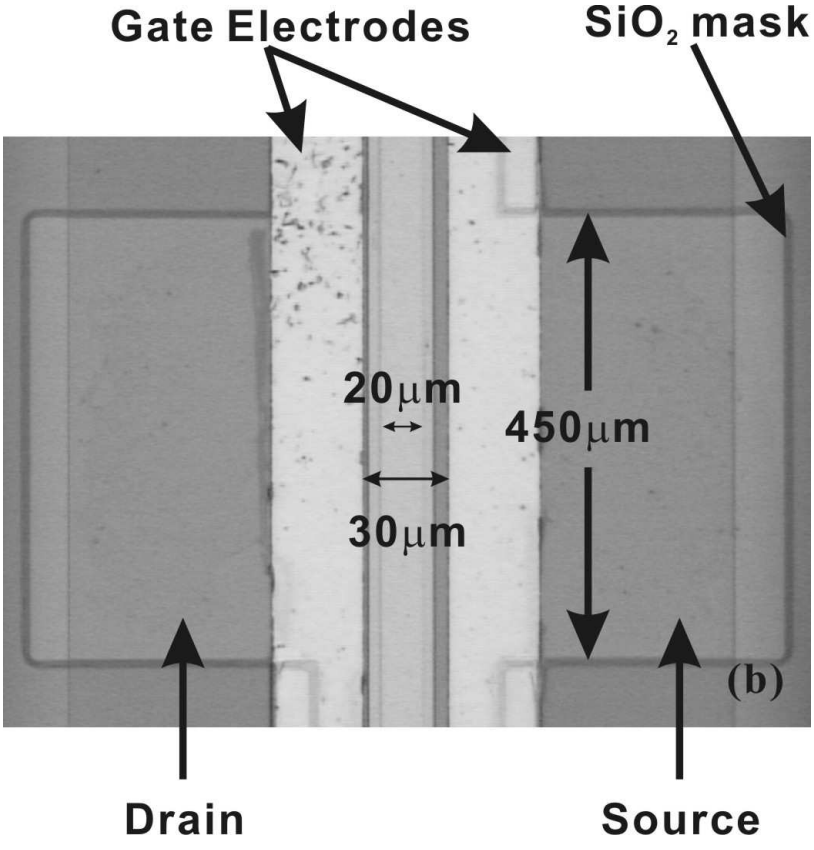


(b)

Figure 2.7: Photograph of the chip with dimensions as indicated. (a) A single IGFET/OFET module whose gate areas is defined by PSR400BN epoxy cells. (b) Detail of the gate area with two Au electrodes separated by 30 μm.

to define the contact area between the OS and Au to limit more precisely the geometry of the conducting path for the measurement of the conductivity of OS (Fig 2.7(b)).

2.2.2 Organic semiconductor preparation

Two conducting polymers are used in this studies, Poly-(phenylenesulfidephenyleneamine) (PPSA) and polyaniline (PANI). Polyaniline was purchased from Aldrich in the form of emeraldine base with a molecular weight of 2×10^4 D, it is dissolved in formic acid, the concentration is $\sim$ 1mg/mL. PPSA sample was prepared by Klaus Müllen *et al.* at the Max-Planck-Institute for Polymer Research, Germany.[12,13] PPSA cast solution is made by dissolving PPSA in cyclohexanone, the concentration is $\sim$ 5 mg/mL. Conducting polymer solution was casted into the epoxy cell of the IGFET/OFET module. After the casting, the test platform is vacuum dried for 15 min to get rid of the influence from solvent.

The solvent casting of OS results in a film of nonuniform thickness across the cell, which is due to the formation of a meniscus at the cell walls. However, the thickness of the OS film is relatively uniform between the Au leads, in the region defined by the SiO_2 mask.

2.2.3 Electrical instrumentation

GT03 test platform is attached to a 28-pin DIP ceramic header (Edison engineering Inc.) with silver-based conducting epoxy, then wire-bonded to the header with gold wires. Transistor characteristics were measured with HP 4155A parameter analyzer together with HP 16442A test fixture.

2.3 Chemical effects on organic semiconductor bulk properties

Conductivity is one of the most important properties of organic semiconductors. Many organic electronics operates based on the principles that the conductivity of OS can be modulated by chemical environment. And on principle, Organic Field-Effect Transistor (OFET) can also be treated as a resistor that the resistance is modulated by the externally applied gate voltage. Conductivity is a function of both the concentrations, n, and the mobilities, μ, of the charge carriers

$$\sigma = e(n_n\mu_n + n_p\mu_p) \tag{2.5}$$

In the equation above the subscripts n and p represent electrons and holes, respectively. The external environment affects both properties. The carrier concentrations can be changed by the interactions of the OS with electron donor/acceptor gases, i.e., by formation of a charge-transfer complex. Whether the OS acts as an electron donor or electron acceptor and what fraction of charge δ is transferred depends on the position of the Fermi level of the OS relative to the Mulliken electronegativity of the guest gaseous species.[43–46] In that respect the gas is treated as a secondary dopant.[47–50] Thus, if the electron affinity of the guest gas is lower than that of the host matrix, an electron is transferred from the gas to the OS and vice versa. The shift of the Fermi level, ΔE_F, resulting from this charge transfer is related approximately to the partial pressure, P_G, of the host gas present in the mixture of background gases ΣP_j[51]

$$\Delta E_F = const. + \frac{kT}{2\delta} ln(P_G + \Sigma P_j) \tag{2.6}$$

Most of the OS used in organic electronics are p-type materials, the major carrier in it is holes. When it interacts with electron donors, the density of holes are lowered and this leads to lowering of their conductivity, according to eq 2.6. That effect has been utilized in the design of chemical sensors called chemiresistors in which conducting polymers form the selective layer of the sensor.[36,52,53] As an example, the effect of ammonia on the conductivity of undoped PANI is shown in Fig 2.8. When GT03 test platform is connected in the OFET configuration without applied any gate electrical field, it works as a chemiresistor in fact. By applying voltage at the gate metal electrode and measuring the current, we can plot the $I - V$ or the OFET $I_D - V_D$ characteristics (Fig 2.8). The reciprocal of the slope is the resistance of the OS film. The resistivity of undoped PANI estimated from these measurements is approximately $\rho = 1.8 \times 10^5$ Ωcm, increasing 100% upon exposure to ammonia. Ammonia molecule is a typical strong electron donor, it has a lone electron pair and can strongly combine with p-type such as PANI. PANI based chemiresistor has already been used for detection of gases similar to ammonia.

The relative change of conductivity upon exposure of the OS to NH_3 illustrates the chemical effect on bulk conductivity of this material. It should be noted that even though we used the OFET configuration for the measurement, but no actual field-effect was observed on this PANI based OFET partly because PANI has a very high density of carriers in bulk, it is very difficult to modulate PANI thought the gate electrical field to make the transistor "off". So in this measurement, only a ohmic dependance of current on applied V_D is observed. Other materials like poly(3-hexylthiophene)[54] shows good field-effect on this test platform which we will discuss in the later chapter.

The mobility, μ, can also be affected by interaction of the gas or vapor with the OS, which causes its swelling.[38,55,56] In this case the carrier hopping distance is affected, i.e.,

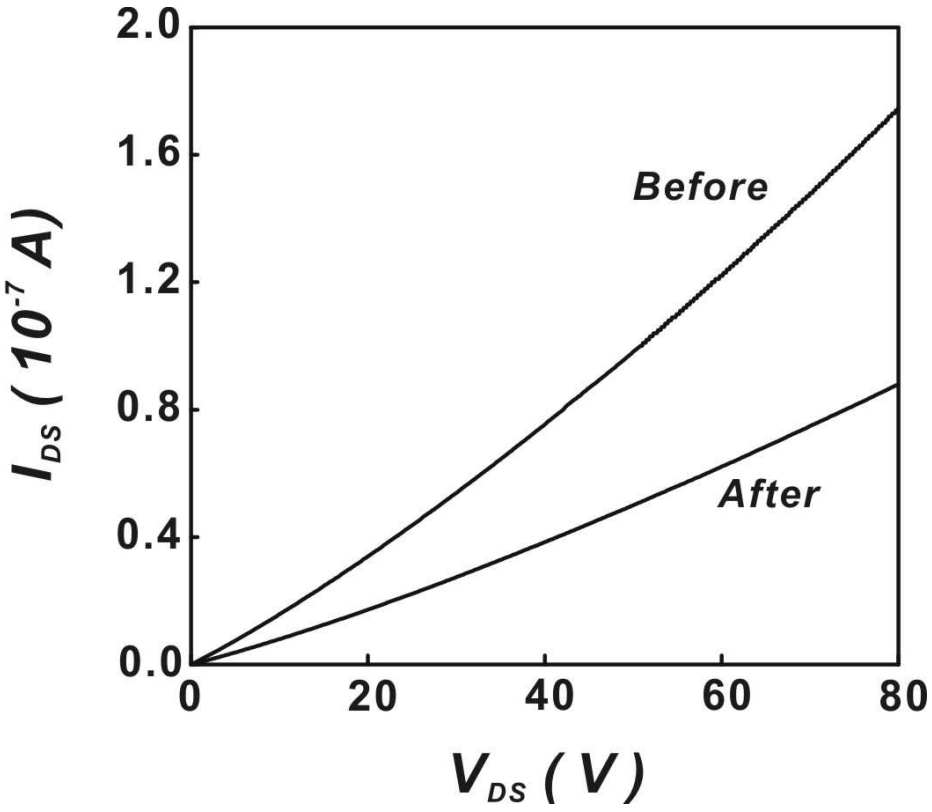


Figure 2.8: Effect of ammonia on OFET characteristics of undoped PANI: before and after exposure to ammonia (1000 ppm) in nitrogen. The scan rate was 316 mV s^{-1} and the gate voltage $V_G = 0$ V.

the mechanism of response of certain chemiresistors, but, to our knowledge, it has not been considered as being important in other forms of organic electronics.[38,52,53]

Work function (WF) is another key property of electronic materials that impacts their use in solid-state devices. Work function for organic material is also called electron affinity, it is defined as the energy required to remove an electron from the Fermi level of the material and deposit it in the vacuum reference level, which lies outside the electrostatic field of that phase. The work function of a single material is not experimentally accessible. However, the difference of the WF of two materials can be measured by a variety of methods of which the vibrating capacitor (Kelvin probe) or a field-effect transistor (also a capacitor) are the best known.[57] The difference of the WF enters this discussion in two places. First, the difference of the WF of silicon and OS affects the threshold voltage of devices that rely on the semiconductor field-effect. Second, it affects the quality and type of contact between OS and metal in the OFET.

The chemical modulation of the WF of OS has been successfully utilized in chemically sensitive field-effect transistors (ChemFET) for detection of gases according to equation 2.6 ,[43,58] In the previous chapter, the relationship between WF change and the shift of threshold voltage (V_T) of ChemFET has been described. In Fig 2.9 shows an example of how ChemFET with PANI as the sensing layer is used for detecting the ammonia. The GT03 test platform is connect in "so-called" source-follower configuration as shown in Fig 2.10. In this configuration, the gate electrodes are connected with the drain electrode, a constant current is feeding through the drain electrode using a custom designed electrical circuit board. When the ChemFET works in the saturation region where $V_D < V_G - V_T$, it follows the equation 2.2. Since I_D is kept constant, and V_T changes according to the PANI WF change on exposure to NH_3, so the measured voltage signal V_G change is an indication

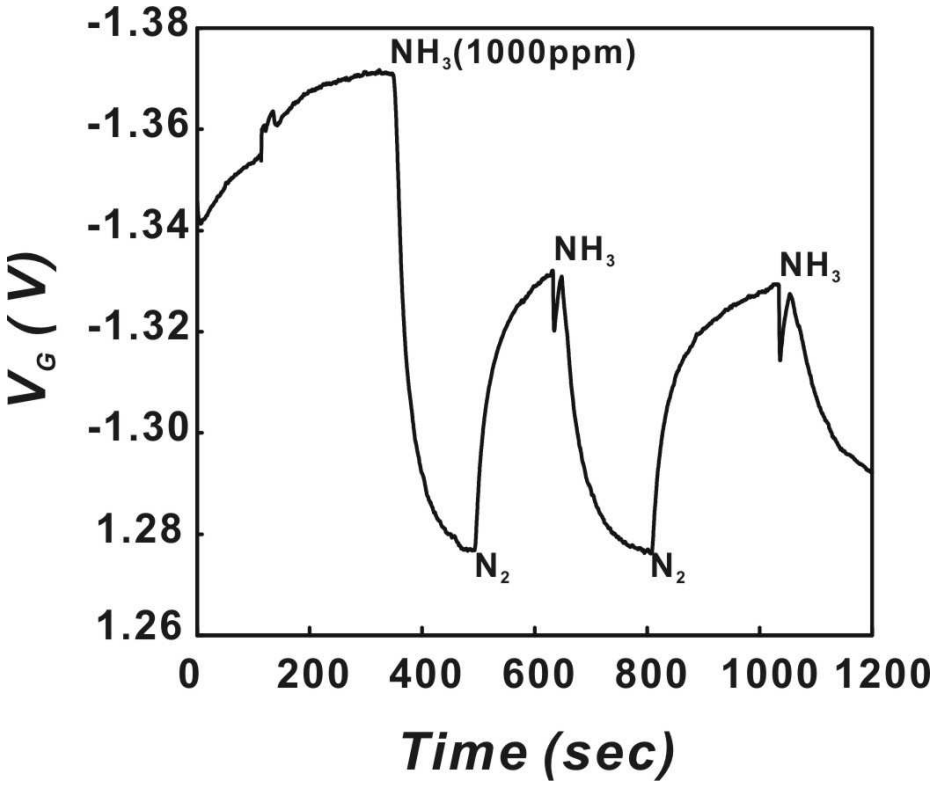


Figure 2.9: Response of ChemFET with undoped PANI to ammonia (1000 ppm) in nitrogen. The ChemFET is connected in source-follower configuration, and the constant drain-source current $I_D = 200$ μA.

of the exposure to NH_3, and ΔV_G can be calibrated to the concentration of the NH_3 gas.

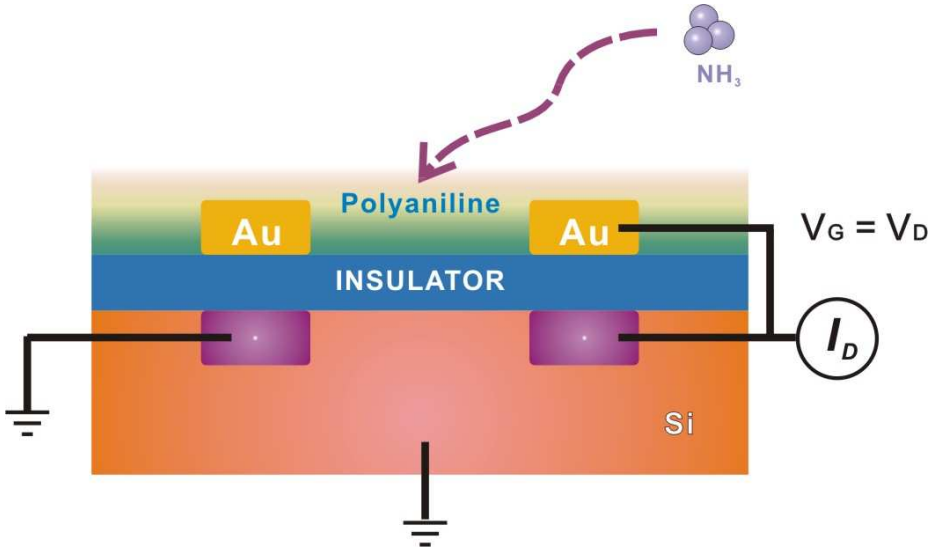


Figure 2.10: Schematic diagram of source-follower configuration of test GT03 test platform for gas sensing.

2.4 Chemically induced effects at the organic semiconductor/dielectric interface

The fact that surface conductivity of the dielectric substrate can have a detrimental effect on the performance of solid-state electronic devices has been recognized for 40 years.[59] The main problem is the surface conductivity forms a parasitic pathway of current which is a big interfere in electrical measurements. Oxide based insulating substrates (e.g., glass, quartz, sapphire, etc.) can easily absorb chemical species in ambient environments. It is known that the surface conductivity of the oxides changes with the amount of sorbed water, making water the most common interferant for devices that are operated at room temperature and in ambient atmosphere.[60–65] Other amphiprotic molecules, such as alcohols, organic acids, amines, etc., can chemisorb on such surfaces and increase their interfacial conductivity. The chemisorbed water is difficult to remove, and heating in a vacuum above 100 °C is usually required to minimize the effect of surface hydration.[66] At the relatively

high voltages that are used for operation of some devices, the electrolytic decomposition potential of hydrated oxides at the interface of the metal contact and the hydrated surface of the insulator is easily exceeded, leading to electrolytic decomposition at the interface. When the parasitic current becomes comparable to the current flowing through the OS, interpretation of the results becomes problematic.

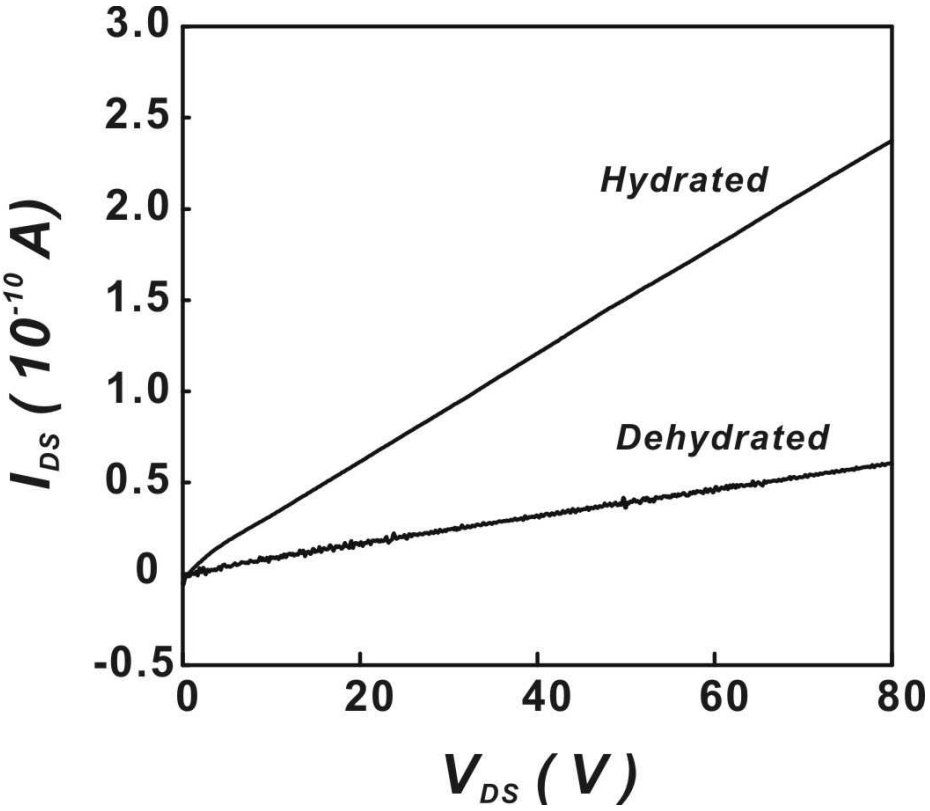


Figure 2.11: Effect of parasitic conductance due to the hydration of the interface between OS and silicon (oxy)nitride in the OFET mode. PPSA is used as the OS, I_D = 0V. Device is hydrated in water for 10-15 min, and is dehydrated in a vacuum oven at 88 °C for 12hr. Scan rate = 1 V s^{-1}.

The materials used for OFET usually have very low conductivity, it is necessary for OFET because that helps the OFET to have the "off" state. Under this situation, the danger of creating a competing parasitic conductive pathway that parallels the conductance through the OS is very real. In Fig 2.11 the current flowing through an undoped (i.e., highly

resistive) OS is compared for a (1) "hydrated" and (2) "dehydrated" device, operated in the OFET mode. When the adsorbed water is removed from the interface, the measured resistance decreases by 75%. Similar measurements were made also in the IGFET mode, with the chip that had no OS in the gate region. If the interface is conducting (i.e., wet), it is possible to apply common V_G to both Au electrodes and thus obtain regular IGFET characteristics (Fig 2.12, curve 1). However, when the interface is dry (i.e., nonconducting), the device behaves like a normal "floating gate" IGFET (Fig 2.12, curve 2) and no drain current modulation is possible. There is no effect of hydration when an OS is deposited over a wet or dry interface. In this case molecules adsorbed at the interface affect the threshold voltage of the IGFET only by their dipolar contribution to the electric field.

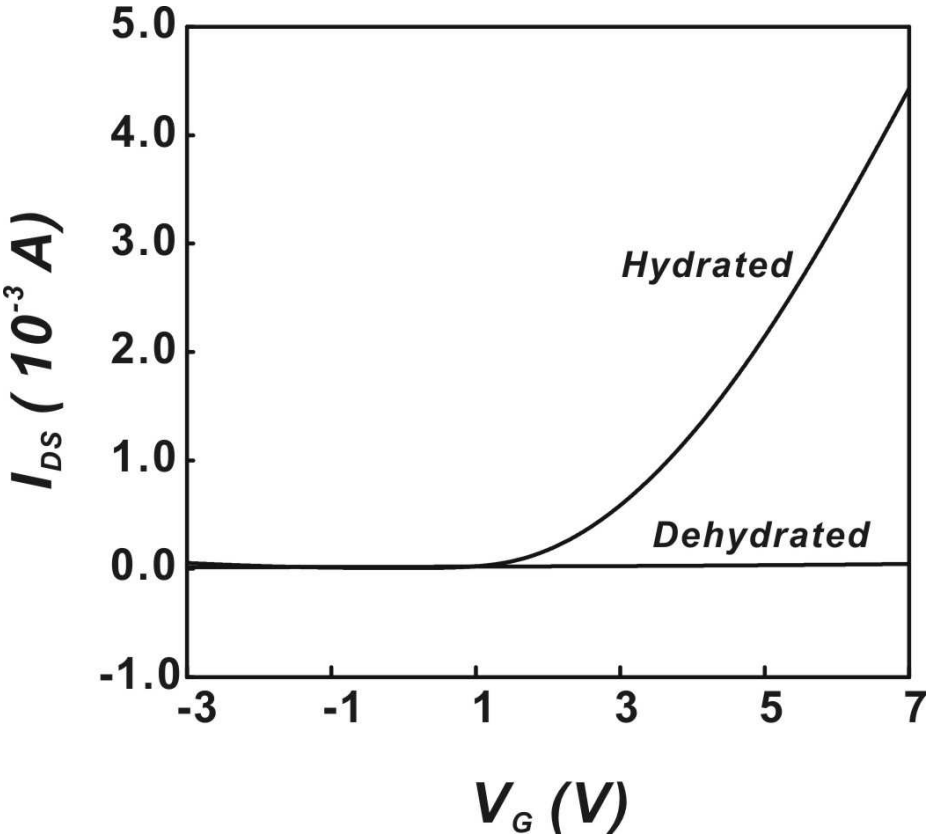


Figure 2.12: Effect of hydration on IGFET mode of operation. No OS is deposited on the silicon (oxy)nitride. $V_D = 5$V at 100 mV s^{-1}. Device is hydrated in water for 10-15 min, and is dehydrated in a vacuum oven at 88 °C for 12hr.

Interfacial currents following other parasitic pathways at the wire-bonded devices may be also observed. They depend on the specific geometry of the device, how it is connected to external instrumentation, and the materials used. Obviously, when a high voltage, on the order of tens of volts with respect to ground, is applied to any contact, different parasitic leakage current pathways may be created. This is particularly true when a high voltage is applied to the OS, which itself has a very low intrinsic conductivity.

Another type of leakage current is due to the dielectric breakdown of the gate insulator under high applied electrical field. In the case of a silicon dioxide/silicon nitride gate insulator, such leakage, also known as "punch-through", occurs when the electric field exceeds 105 V cm^{-1}. For this reason, the applied gate voltages in silicon transistors are rarely higher than 20 V. It is not possible to predict when such failure may take place because it depends on the types of materials used, the density and location of the defects, and the geometry of the device. In our OFET/IGFET platform the gate failures have sometimes occurred at $V_G > 60$ V.[67] The presence of gate leakage currents can and should be always measured and reported. As the general rule, the sum of the leakage currents should not exceed 0.1% value of the measured I_D.

2.5 Chemical effects on organic semiconductor/metal contact

The physics of charge carrier injection through an interface separating a metal and an organic material strongly depends on the equilibrium dark conductivity of the OS. In undoped OS the density of free charge carriers is very low, exhibiting insulating behavior. Therefore, the Schottky depletion region cannot be formed at a metal/OS interface. The

conductance in an ideal insulating film is assumed to be zero. However, low doped semiconductors, just like real insulators, show carrier conduction when the electric field or the temperature is sufficiently high. Table 2.13 summarizes the basic conduction processes in organic semiconductor/metal contacts.[39] For a given contact, each process may dominate at certain temperature and voltage ranges and these processes are also interrelated.

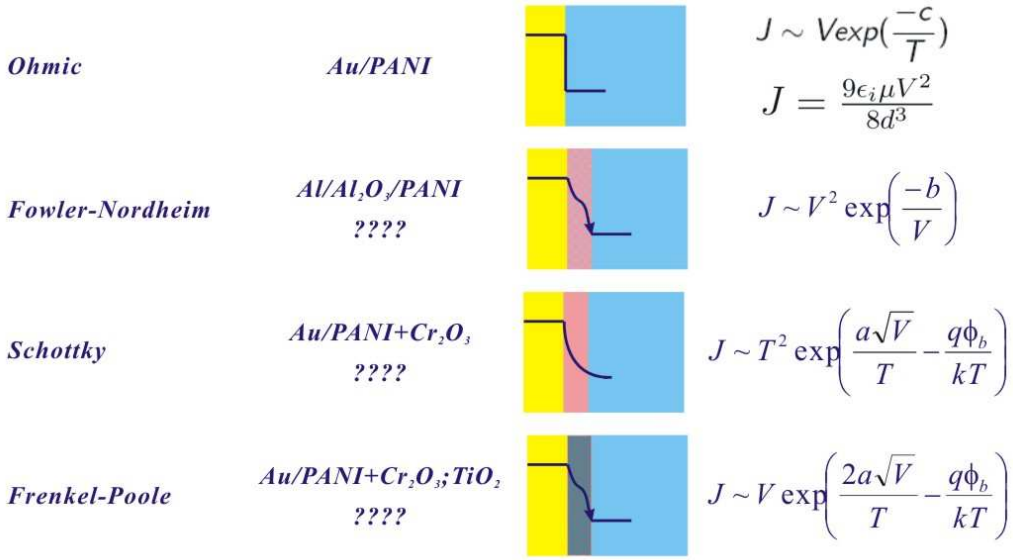


Figure 2.13: Four types of contacts encountered in organic electronics. ???? represents impurities.

2.5.1 Ohmic contact

For efficient operation of the device, the contacts must be ohmic. If this is not the case, there is a limitation depending on the nature of potential barriers existing at the contacts that can be controlled by energy barriers across the ohmic metal/ OS interface.[68] Although contact potential exists at the ohmic metal/OS interface, it is not subject to chemical modulation and the applied voltage falls across the bulk of the OS. The charge-injecting electrode has no significant resistance and is able to supply any current required by the bulk. When such contact is made to an undoped organic semiconductor, which has no free

carrier density, the current is limited by bulk space-charge effects which result from carriers injected into the undoped polymer, where no compensating charge is present.[69] Modelling shows that for ohmic contact between metal and low-mobility OS, the barrier to carrier injection has to be lower than about 0.3-0.4 eV[70,71]

Gold and indium-tin oxide (ITO) are commonly used to form an ohmic contact with most of the p-type OS. The electrical properties of ITO vary considerably with chemical composition and processing history. Work functions determined by different measurements vary from 4.0 to 5.2 eV for a range of commercial ITO samples.[70] This is in agreement with measurements which show that ITO with WF of 4.8 eV forms an ohmic contact with an OS with an ionization potential Ip = 5.1 eV but a blocking barrier contact with a OS with Ip = 5.4 eV.[72,73]

The work function of gold has been assumed to be about 5.0-5.2 eV. Several studies show that the work function of several commonly used π-conjugated materials is about 5 eV. In this case, the barrier between the p-type polymer and gold is relatively small, representing a quasi-ohmic contact, with a symmetrical and linear current-voltage dependence.[74–78] Nevertheless, the experimental contacts are sometimes rectifying, indicating a higher WF of the OS than that of gold.[78]

2.5.2 Barrier contact

In general, dark carrier injection over a barrier into insulators, i.e., undoped organic semiconductors, follows the Richardson-Schottky and Fowler-Nordheim models. The former deals with thermally activated over-barrier injection; the latter emphasizes the tunnelling charge injection through a triangular barrier.[79] Analysis of high work function metal/OS interfaces shows that the I-V characteristics depend not only on the applied voltage but

also on the electric field at the contact, the temperature, and impurities. This clearly points to a tunnelling model for carrier injection in which the carrier is field emitted through a barrier at the electrode/OS interface.[80] These barriers may be caused by interaction of the OS with the metal, interaction of both with ambient air, e.g., by metal oxide formation, or over-oxidation of the OS. The last three are chemical by nature. They change the local band structure of the OS/metal interface. They may also offset the energy bands at the interface and the electrode through which holes and electrons are tunnelling when the applied electric field tilts the OS bands.

It is obvious that the current-voltage characteristics are sensitive to the barrier height. Since the current density depends on the applied voltage, we can see that increasing the barrier height, even slightly, leads to an exponential decrease in current (Table 2.13). This type of charge transport is considered to occur under high electric field in both undoped OS as well as metal oxide layers, e.g., Al_2O_3 and Cr_2O_3. (Table 2.13)

Chemical modulation of the barrier can occur in different ways depending on the chemical properties of the contact materials. This modulation involves contamination of noble metal surface by metal oxides or aging of low WF metal electrodes, such as chromium, silver, or aluminum. Since metal oxides have a lower WF than the parent metal, those changes can be in the range of several hundreds of milli-electronvolts. The resulting charge carrier injection rate can vary by several orders of magnitude.

Molecular modelling which includes specific chemical reactions between the metal and the OS has been done.[81–84] On the basis of such calculations, it has been postulated that the metal plays an important role in determining the extent of charge transfer at the metal/ OS interface: Ca and Na appear to transfer charge at the interface without significantly altering its chemistry.[67,81] However, these low-WF metals are notoriously unstable in air.

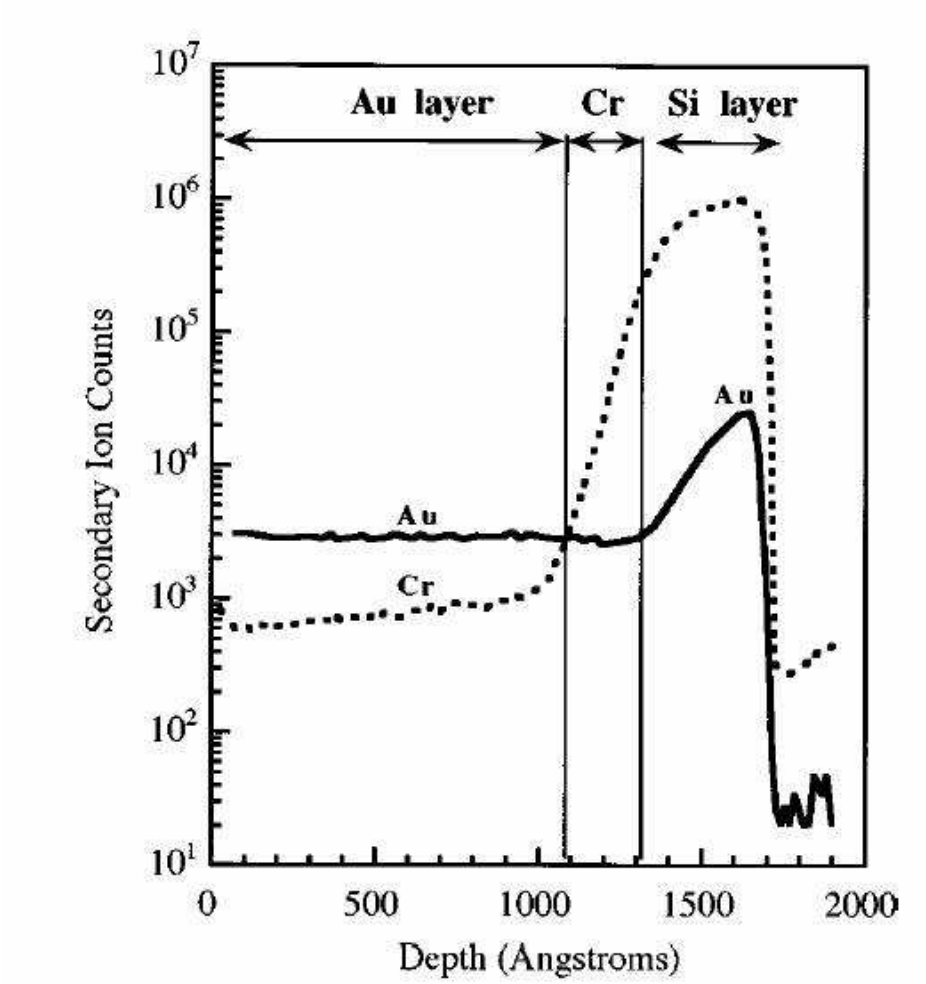


Figure 2.14: Depth profiles of atomic composition of Au/Cr/Si contact obtained by time-of-flight secondary-ion mass spectrometry. Note that Cr is present both within and at the surface of the Au. (Reprinted with permission from ref.[1] Copyright 1998, American Institute of Physics.)

Gold forms ohmic contact with most p-type OS layers. In OFETs utilizing Au bottom electrodes, over which the OS is deposited, the current density shows a linear dependence on the applied electrical field, indicating an ohmic behavior, as long as no "glue metal" is used to increase the adhesion of Au on the substrate. A non-ohmic behavior can be observed, and the hole injection efficiency is significantly degraded when Au is evaporated onto Si using a thin Cr adhesive layer. The severe depression of the hole injection efficiency from the Au/ Cr substrates appears to be associated with the known contamination of the Au surface by Cr at the OS/metal surface.[1] The chromium atoms migrate along the grain boundaries of polycrystalline Au to the surface of Au and form Cr_2O_3 at the Au surface. This contamination affects the surface properties of the noble metal by lowering its WF. A depth profile (Fig 2.14) of an Au/Cr/Si layer by TOF-SIMS shows the presence of chromium atoms within and at the surface of the Au substrate.[1]

The contamination effect can be generally observed for glue metals as well as for barrier metals, used for deposition of thin films of noble metals on oxide surfaces. The surface contamination of the noble metal layer is an ongoing process affected by several parameters, namely, temperature, grain size of the noble metal, and degree of oxidation of the glue/barrier metal. It affects the long-term behavior of the contacts and is known as "contact aging". Interestingly, response of OFET with (undoped) PANI as the OS to chloroform has been interpreted as a "semiconductor field-effect" response.[85] In that report Au/Cr/SiO2 contact was used. The reported I_D-V_D curves have characteristics of high serial contact resistance, indicating that it is the modulation of the contact resistance that is responsible for the observed effect.

The method of choice for metal contact deposition in organic devices, such as light-emitting diodes or thin-film transistors, is evaporation.[86] However, the nature of the electrical contact can be affected by chemical damage to the OS during that process. The contact properties of a metal evaporated on top of the OS can differ markedly from the contact properties of the same metal when the OS is coated onto a bottom metal electrode. It has been observed that the presence of a blocking interface in the top contacts is not consistent with the estimation of the injection barrier height from the relative WF of the interface components.[1,87] This observation is not unique to an Au/OS interface, having been confirmed also for evaporated Ag and mechanically made liquid Hg contacts.[87] The nature of evaporated Au top electrodes and the possible damage to the OS can vary with the number of deposition steps and evolve from blocking to ohmic with time and temperature.[1,87] This is attributed to the physical or chemical changes of the organic material at the interface during the metal deposition.

Another source of the barrier formation at the electrical contact in organic devices is due to the changes of the electronic properties of the OS when it is stored in ambient atmosphere. Water vapor irreversibly reduces the density of trapping and doping states in the band gap.[88] The combined effect of oxygen and water at the contact can cause irreversible over-oxidation and formation of organic carbonyl groups at the conjugated polymer. When that happens the π-electron system is interrupted, resulting in reduced carrier mobility.[89]

Poly(3-alkylthiophenes) are solution-processable semiconductors with the high charge-carrier mobility reported. Practical use of this class of semiconducting polymers, however, is restricted by their limited stability in air and light, due to oxidative doping.[90] A reversible effect of oxygen on structures based on poly(3-alkylthiophenes) has been observed.[4,88,91]

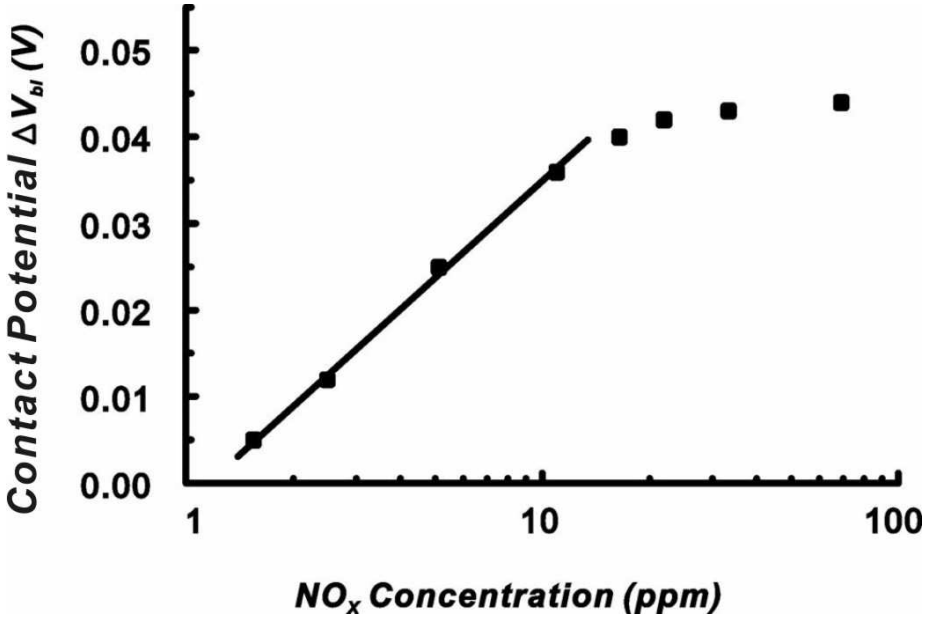


Figure 2.15: Gas-induced change of the contact barrier characteristics of a PPy/Au metal junction as a function of NO_x vapor concentration in ambient air.[2]

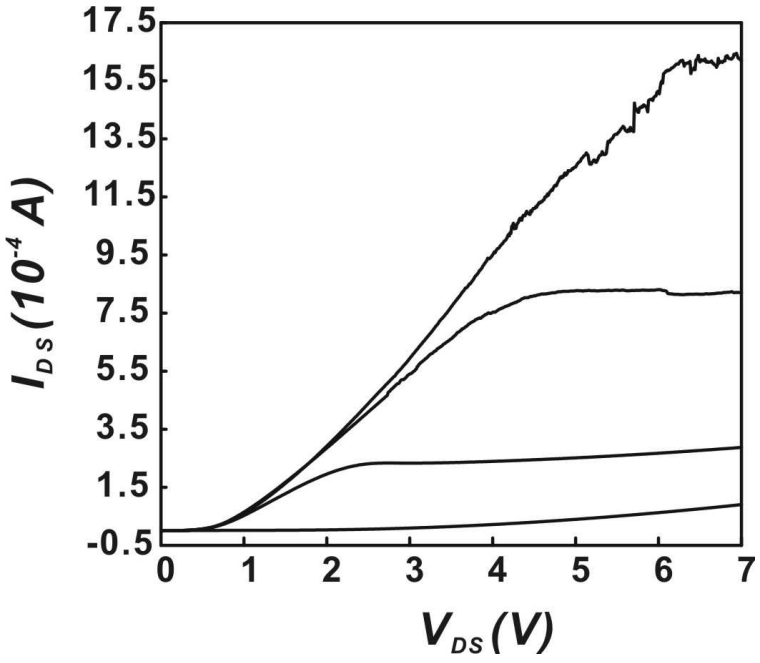
Oxygen induces acceptor states and fills the traps in the band gap. Analysis of poly(3-hexylthiophene) field-effect transistors shows that the extent of the reversible modulation of electronic properties is proportional to the oxygen partial pressure.[4] In the absence of oxygen, a typical FET-like response is observed, i.e., clear saturation currents, which are proportional to the gate bias. In the presence of oxygen, the current increases by an order of magnitude, the charge carrier mobility is lowered by the formation of the charge-transfer complex, and the curves take on considerable "ohmic" behavior. These I-V curves are fully reversible upon removal or addition of oxygen.

Studies of the effects of ambient atmosphere on contacts have focused mainly on oxygen. However, the effect of other gases has been documented, mainly from the sensing point of view.[92] Fig 2.15 shows the dependence of the change of the contact potential of a polypyrrole/Au metal junction on the NO_x concentration. It can be clearly seen that the

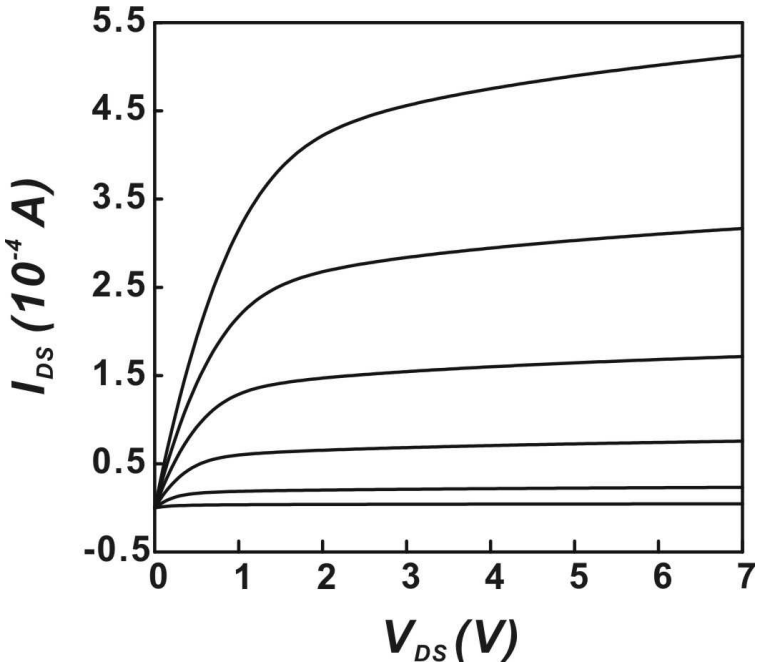
change of the contact potential is exponentially dependent on the NO_x concentration, indicating the dependence of the WF on the charge-carrier concentration according to equation 2.6.

Semiconductor/metal interfaces form the basis of many rectifiers, point contact diodes, metal-semiconductor field-effect transistors, surface barrier chemical sensors, and other surface junction devices. In practice, even if all WF (Fermi levels) were matched exactly to the highest occupied molecular orbital (HOMO) or lowest unoccupied molecular orbital (LUMO) levels, there exists a finite probability of having potential barriers at all junctions possibly due to surface states, impurities adsorbed during junction formation, and possible chemical reactions between the materials contacted. In principle, these junctions behave as parasitic nonlinear resistances in series with the linear source and drain access resistances. Their effect on the shape of the $I_D - V_D$ and $I_D - V_G$ characteristics is shown in Fig 2.16(a) and Fig 2.17(a), respectively. The distortions are clearly evident from comparison with normal IGFET characteristics shown in Fig 2.16(b) and 2.17(b).[29,93] It is obvious that transistors with serial contact resistance do not follow the ideal curves, given by equation 2.1, 2.2.

The presence of contact resistances and their effect on the transistor characteristics have to be considered when developing OFET in order to interpret nonlinearities in the current-voltage characteristics correctly. The IGFET/OFET platform discussed in this chapter allows one to distinguish between the field modulation of the semiconductor resistance in the gate channel and that of the metal/OS source and drain contacts. It can help to optimize the OFET with respect to the quality of contacts and to study and improve independently the electronic properties of the OS layer.

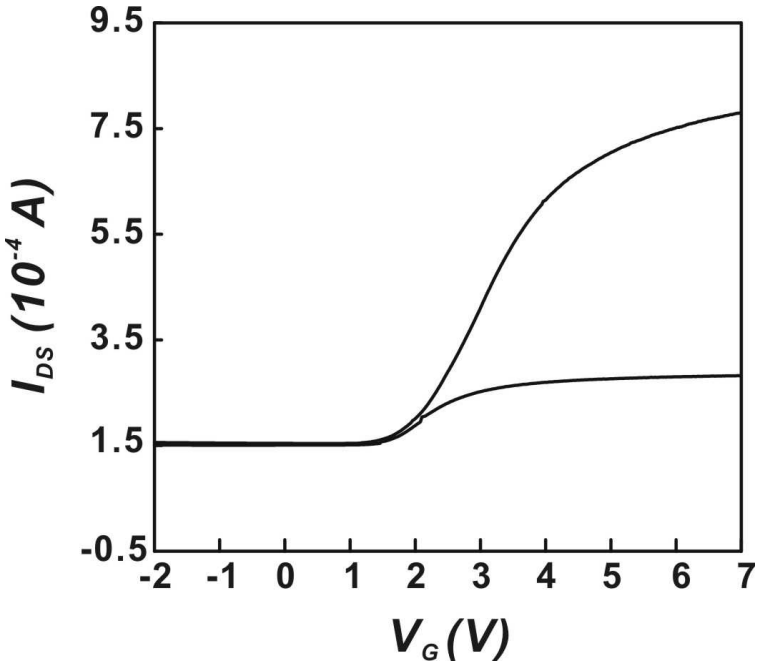


(a)

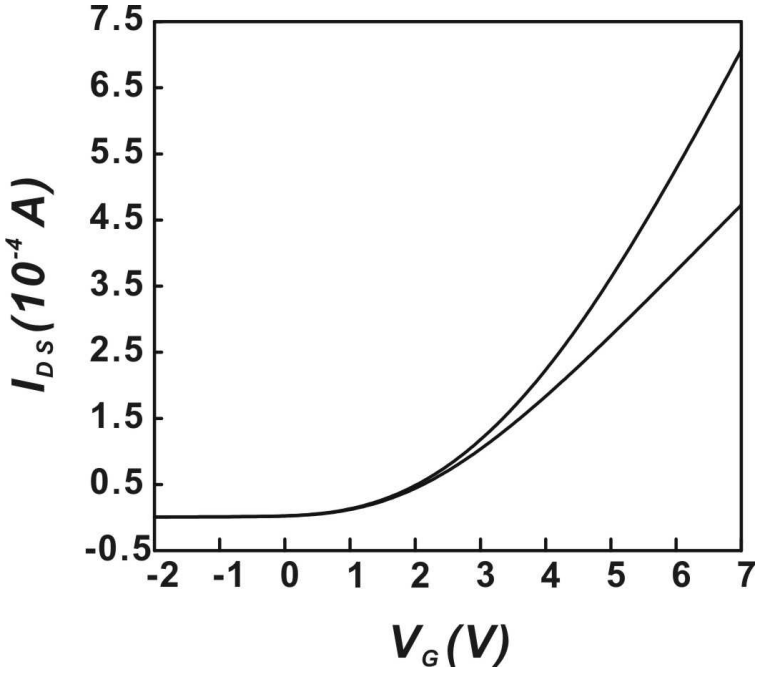


(b)

Figure 2.16: Comparison of $I_D - V_D$ characteristics of silicon IGFET (a) with contact resistance, V_G: 0∼6V step 2V (b) without contact resistance, V_G: 0∼5V step 1V . The contact resistance was formed by a layer of SiO_2 at the Si/Ti,W/Au contact.



(a)



(b)

Figure 2.17: Comparison of $I_D - V_G$ characteristics for the same IGFET (a) with contact resistance V_D = 1V, 2V and (b) without contact resistance V_D = 1V, 2V.

2.6 Conclusions

Most of the chemical effects in organic electronics come from oxygen and water, although other minority components in the ambient atmosphere can affect the organic electronics just as well. That phenomenon is utilized in solid-state gas sensors that use the same or similar OS. Some of those effects are reversible, i.e., secondary doping of bulk of the OS with oxygen, but some are irreversible, i.e., formation of barrier oxides on metal contacts. Since oxygen and water are the major components of ambient atmosphere, they always have to be taken into account when designing, fabricating, and testing organic electronic devices.

Organic electronics is a new technological area that attracts a great deal of attention. It promises to offer a wide range of interesting applications that would be complementary to but otherwise not attainable with conventional silicon electronics. The importance of understanding and controlling the chemical environmental factors is critical for both solid-state chemical sensors and organic electronics intended for signal and information processing. Failure to do so may result in experimental artifacts, and incorrect allocation of developmental resources. It is particularly important in organic electronics in which the OS are subjected to high applied voltages that are close to the breakdown limits of many materials and structures. Such breakdowns increase the danger of parasitic current pathways that may lead to misinterpretation of some measurements. To diagnose this risk, a new test platform GT03 has been developed that allows direct comparison of performance of the OS in the OFET as well as in the IGFET configuration.[94] Its function in the context of the chemical effects is described also in this chapter. It is clear that the importance of performing a baseline test, particularly measurements of various parasitic leakage currents, should not be underestimated.

CHAPTER III

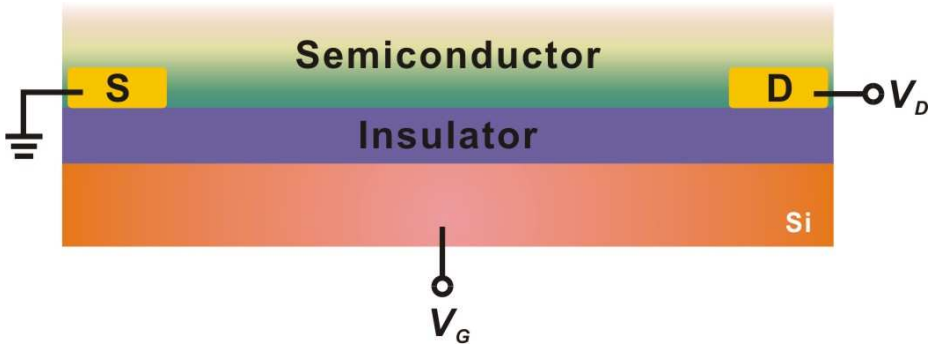
CHARACTERIZATION OF CONTACT MODULATION IN ORGANIC FIELD-EFFECT TRANSISTORS

3.1 Introduction

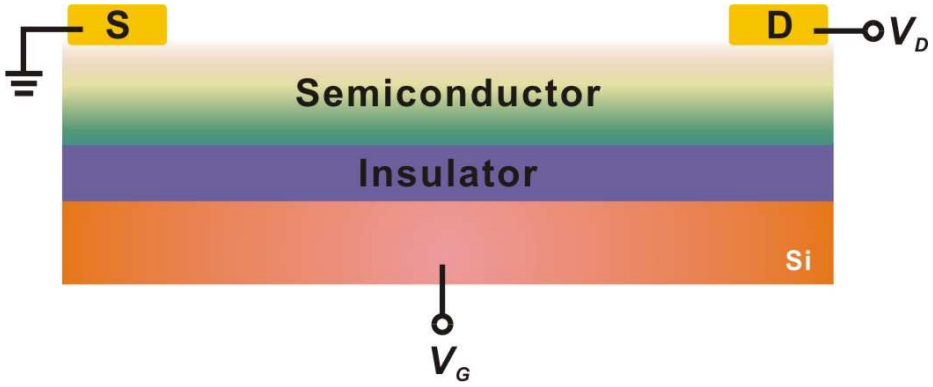
Organic Field-Effect transistor (OFET) has become one of the most important organic electronics. The idea of OFET was first described by H. Koezuka and his co-workers in 1987.[95] Now it has been the focus of research in recent year and there has been an explosion of the reports OFET.[96–101] OFETs have many advantages over conventional silicon technology: they can be fabricated at low cost, large area coverage, and because organic compounds can be processed at low temperature, it offers the opportunity of integrating organic electronic devices on inexpensive flexible plastic substrates. The applications of OFETs include switching devices for active-matrix flat-panel displays (AMFPD), low-end display driving circuits, low-end smart cards and electronic identification tags, and etc. Additionally, organic integrated circuits and all-polymer integrated circuits have been demonstrated.

3.1.1 Fundamentals of organic field-effect transistors

Typical OFET structure is displayed in Fig 3.1. The main components of OFETs are source drain and gate electrodes, a dielectric layer and a semiconductor layer. OFETs have two configurations as shown in Fig 3.1, bottom-contact where the semiconductor layer is sitting on top of drain source electrodes; top-contact where the drain source electrodes



(a)



(b)

Figure 3.1: Schematic diagrams of device configurations of OFETs (a) bottom-contact configuration (b) top contact configuration.

are sitting on top of the semiconductor layer. The distance between the drain and source electrodes is defined as the channel length (L), and the length of the drain source electrodes is defined as the channel width (W). The current flows between the drain and source electrodes is modulated by the voltage applied at the gate electrode. When no gate voltage (V_G) is applied, the drain current (I_D) is very low and the transistor is normally off. When the gate voltage increases, charge carriers can accumulate at the interface between the semiconductor and insulator. Then the drain current increases due to the increased charge carriers and thus the transistor is turned on. This is a very simple description of the operating principle of OFETs.

An analytical model has been suggested by Gilles Horowitz for organic based thin-film transistors.[102–104] The main principle of the calculation was based on the gradual channel approximation.[39] Gradual channel approximation is usually applied when the electrical field along the channel is much smaller than in across it. In the real OFET device case, the channel length is much larger than the thickness of the semiconductor layer, so it can be simulated with a one dimensional equation along the channel dimension. In this analytical model, several assumptions have been made: first, the charge mobility of the semiconductor is constant, second, the density of free carriers and that of dopant are equal. From the calculations, equations very similar to silicon based conventional transistor are evolved.

In the linear region, where $V_D < V_G - V_T$,

$$I_D = \frac{\mu C_0 W}{L}\left[(V_G - V_T)V_D - \frac{V_D^2}{2}\right] \tag{3.1}$$

Here V_T is defined by Equation 3.2

$$V_T = \pm\frac{qn_0d_s}{C_0} + V_{fb} \tag{3.2}$$

In the equations above, the μ is the charge carrier mobility, C_0 is the unit capacitance of the dielectric, V_T is the extrapolated threshold voltage, n_0 is the density of free carriers, and the d_s is the thickness of the semiconductor, V_{fb} is the flat band voltage and q is the unit charge, "+" sign is used for p-type OS and "-" sign is used for n-type OS.

When $V_D > V_G - V_T$, the accumulation layer near the drain change to a depletion layer. It is assumed that the accumulation layer extends from the source up to a point where the gradient voltage drop in the drain electrical field equals V_G, beyond which it is replaced by a depletion layer.

$$I_{dsat} = \frac{\mu C_0 W}{2L}\Big(V_G^2 - 2V_TV_G + V_TV_p\Big) \tag{3.3}$$

Consider the second assumption mentioned above, the density of free carriers and that of dopant (N) are same $n_0 = N$, the it yields $V_T = V_p$

$$I_D = \frac{\mu C_0 W}{2L}\Big(V_G - V_T\Big)^2 \tag{3.4}$$

V_p is the pinch-off voltage which is defined as the gate bias that applied to an MIS diode, completely depletes the semiconducting layer. ε_s is the dielectric constant, C_s is the unit capacitance of semiconductor.

$$V_p = \pm\frac{qNd_s^2}{2\varepsilon_s}\left(1 + 2\frac{C_s}{C_0}\right) + V_{fb} \approx \pm\frac{qNd_s}{C_0} \tag{3.5}$$

Equation 3.4 is often used to calculate the charge carrier mobility of OFETs through a plot of $I_D^{\frac{1}{2}} \sim V_G$. But it is important to point out that this is based on several assumptions, constant mobility and equal free carriers and dopants density.

There are several parameters in characterizing an OFET, such as the field-effect mobility, an on/off ratio, threshold voltage and subthreshold swing. The field-effect mobility quantifies the average charge carrier drift velocity per unit electrical field, whereas the on/off ratio is defined as the drain-source current ratio between the on and off states. The threshold voltage V_T is a parameter that evaluate the amount of traps. The subthreshold swing S is a measure of how rapidly the devices switches from the off state to the on state in the region of exponential current increase and is defined by $S = V_G/(logI_D)$.

3.1.2 Materials for organic field-effect transistors

The very first OFET was made from polythiophene film, which belongs to the family of the conducting polymers that were discovered in late 1970s.[105] Later the possibility of fabricating organic thin-film transistors (OTFTs) with small conjugated molecules was shown in 1989[106] with sexithiophene an oligomer of polythiophene made os six thiophene rings linked at alpha position. Now, a large varieties of organic compounds have been test for making OFETs, and there are many new materials being synthesized for this purpose.

Currently, most organic materials used in OFETs are π-conjugated organic oligomers and polymers based organic semiconductors. As mentioned above, both polymer and small molecules have been used since the beginning. Conjugated polymers present the advantage of being amenable to specific deposition techniques that have been developed for conventional polymers. Their main drawback is that their performance is still lower than that of small molecules.

As the difference in charge carriers, the organic semiconductors can be classified as p-type and n-type. Both type materials have been used in OFET. In p-type semiconductors, the majority carriers are holes, while in n-type semiconductors, the majority carriers are electrons. Accordingly, the transistor made from these materials are p-type or n-type transistors. n-type and p-type materials are mainly characterized by their high electron affinity and low ionization potential respectively. In the real applications, most investigated organic semiconductor materials are p-type in their non-intentionally doped form. Because of their sensitivity to air and moisture, most n-type semiconductors are not suitable for OFETs, also n-type materials have relatively low field-effect mobilities. Recently, Chua has discussed n-type materials in Nature.[100] Commonly used organic semiconductors include phthalocyanine (PC),[107,108] pentacene,[109] α-sexithiophene,[110] poly(3-hexylthiophene), 3,4,9,10-perylenetetracarboxylic dianhydride (PTCDA),[111] hexadecahalogenated metallophthalocyanines (F16CuPc),[112] etc.

In present stage, almost all devices are made of small molecule semiconductors, especially the pentacene, oligothiophenes and their derivatives. These two material possess the best electronic characteristics by offering high charge carrier mobilities, the mobility reaches 6 cm^2/Vs for pentacene[109] and 1 cm^2/Vs for α-sexithiophene.[110]

Pentacene is an aromatic compound with five condensed benzene rings and has been widely studied for its application in OFETs. Due to its poor solubility of pentacene, pentacene is mainly used in its polycrystalline thin film from vacuum evaporation. The characteristics have been described in many reviews.[104,113] Recently people begin to use soluble precursors to fabricate solution-cast unsubstituted pentacene. the soluble precursor molecules can be converted to pentacene upon heating. Various groups reported works on this

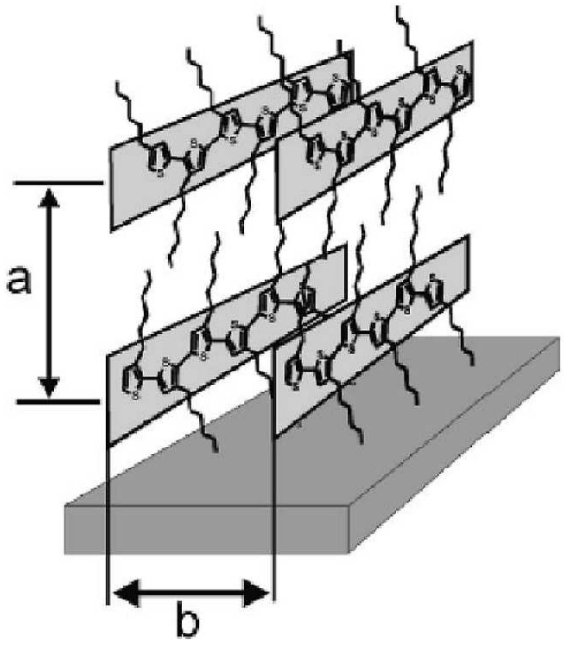


Figure 3.2: Regioregular poly(3-hexyl-thiophene) with edge on orientation of the polymer chains, from.[3]

technique, the mobility of the film can reach 0.89 cm^2/Vs. There are also studies on functionalized pentacene to improve π-orbital overlap for pentacene derivatives, which are still at initial stage.

Oligomers consisting of conjugated oligothiophene and polymers are promising charge transport semiconductors. It is easy to tune their properties by chemical modifications.

There are not many polymer semiconductor materials, the most widely studied polymers in this field are polyfluorene[114,115] and poly(3-alkyl-thiophene) (P3AT). P3AT has attract more attention for its higher charge carrier mobility. Sirringhaus and his coworkers[116] have proved that the performance of the OFETs depends on the chemical structural ordering of the polymer.The structure of the regioregular P3AT is shown in Fig 3.2. The regioregularity plays a very important role here, which makes the polymer highly ordered. Also, the orientation of the polymer chain is another main factor, polymer with the chain edge on has higher mobility.

One reason for polymers to have lower mobility than small molecules is that they have low crystallinity as a result from solution techniques.

In this chapter, we choose regioregular poly(3-hexylthiophene) (P3HT) as the organic semiconductor for our studies. P3HT offers the advantage of good solvent solubility, and it shows good head-to-tail regioregularity. P3HT is reported to gave a mobility of about 0.1 cm^2/V s and current on/off ratio of about 10^6 when processed in an inert atmosphere.[117] When processed in ambient conditions, it exhibited lower mobility and significantly lower current on/off ratio.[118] In this chapter, our purpose is not to study the charge mobility or enhance the functionality of the OFET, so perform all the experiments in ambient air.

3.1.3 Contact resistance in organic field-effect transistors

The main, often quoted attractive features of OFETs which appeal to the " disposable electronics" market are their low fabrication cost, mechanical flexibility and low weight. The low cost is due to the fact that OFETs are usually fabricated in a one-mask lithographic process that does not require expensive mask alignment. Thus, it is claimed that functional field-effect devices can be mass produced by a planar process in which the metal electrodes are printed on flexible dielectric substrates. The deposition of the organic semiconductor (OS) and the realization of the contacts do not require patterning and therefore bypass the alignment step. The final realization of the device then comes out in two basic forms: OFET either with the bottom or with the top metal contacts.

When fabricating the OFET devices in a one-mask process the source (S) and drain (D) contacts lie in the same plane as the OS conducting channel, which is being modulated by the same electric field. This applies both to the top and to the bottom contact devices in which the so called "interdigitated electrode structures" (IDS) are the most popular format.

The purpose of "interdigitation" is to offset the low conductivity of OS used in OFETs, by extending the channel width without appreciably increasing the overall size of the device. Thus, the channel width (W) often exceeds the channel length (L) several hundred times.

The possibility of modulation of the contact resistance by the electric field from the gate electrode in OFET has begun to receive notice in recent years. Because of this complication the application of the IGFET equations for calculating carrier mobilities from co-planar OFETs measurements can be burdened by a major error. In order to circumvent this problem we have designed and fabricated a co-planar structure that allows the separation of the effect of the field modulation of the contact resistances and of the channel resistance. The technique is related to the classical four-point-probe measurement that has been used before for studies of OFETs[119–123] and is a common technique for evaluation of resistivity of thin solid films. Conventional four-point-probe measurements are performed in constant current mode. A small constant current is applied between the external (auxiliary) electrodes and the resulting potential difference between the pair of inner measuring electrodes is used to obtain the resistance of the material. The main objective of such measurement is to eliminate any effect of the contact resistance at the inner electrodes because they are connected to high impedance input and no current can pass through them. That approach assumes that there is linear gradient profile of electric field between D and S. By extending the electric field to D and S, voltage drop at the contacts can be calculated.[39] Our devices operate in related but somewhat different mode that allows us to study the effect of the gate field on both the contact resistances and on the OS bulk resistance. No assumption about the profile of the electric field is necessary.

Another test platform that allows experimental separation of contact modulation and channel modulation has been described previously.[94] It is a typical IGFET in which the

source and drain electrodes have been removed from the gate electric field. However, its preparation requires a multi-mask alignment process and a device fabrication facility that is beyond the reach of most groups engaged in the OFET research.

3.2 Experimental

3.2.1 Test platform fabrication

Interdigitated structure (IDS) was fabricated from heavily doped 4-inch p-type silicon wafer. The gate dielectric consisted of 800 $\mathring{A}$ thermally grown silicon dioxide SiO_2 layer and 800 $\mathring{A}$ LPCVD silicon nitride Si_3N_4 layer. The measured capacitance of this double-layer dielectric is about 56 nF cm^{-2}. The IDS electrodes ($\sim$ 3500 $\mathring{A}$ Au / 300 $\mathring{A}$ Ti) and the back contact layer ($\sim$ 5000 $\mathring{A}$ Au / 300 $\mathring{A}$ Ti) were deposited with E-beam evaporator. The wafer was diced to individual 6.5 mm $\times$ 6.5 mm chips that were attached to 28-pin DIP headers with silver-based conducting epoxy. The wire-bonding was done with gold wires. Before organic semiconductor deposition, chips were first cleaned with isopropanol and DI water, and then in oxygen plasma for 10 minutes

3.2.2 Organic field-effect transistor preparation

Regio-regular poly(3-hexylthiopheny) (P3HT) was used as received. Its molecular mass is about 0.8×10^4 D and it was used without further purification. Casting solution was made by dissolving 4.3 mg P3HT in 5 mL of chloroform:chlorobenzene (3:1) mixture. The solution was drop-cast on IDS chip and dried in air, then put in the vacuum desiccators for at least 30 min to remove the solvent. Film thickness is not uniform across the chip and it varies from 50 nm to 400 nm. A better uniformity can be obtained by spin casting the film but in that mode that deposition requires prior insulation of the exposed, electrically active chip edges in order to prevent formation of a possible leakage path between the OS and the

silicon substrate (gate). Film thickness was measured with Dektak 3^{ST} profilometer.

3.2.3 Electrical instrumentation

Electrical characterizations were performed on a Hewlett-Packard 4155A semiconductor parameter analyzer together with HP 16442A test fixture. In this chapter, we have not investigated the channel length as the parameter and therefore, the variability of the film thickness was less important. Typical experimental parameters of our measurements were: V_{Aux}= 0 $\sim$ -40V with voltage step of 50 mV and the scan rate is 78 mV sec^{-1}. The gate voltage, V_G= 0 $\sim$ -80V with voltage step of 10 V. All measurements were made in dark at room temperature, but under ambient air.

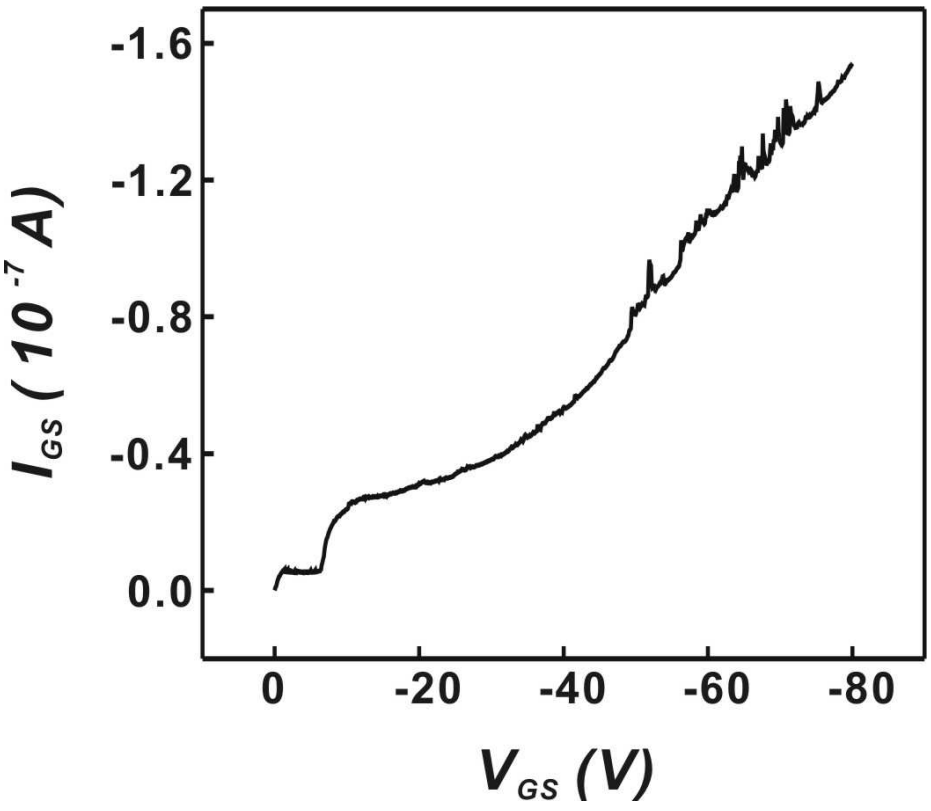
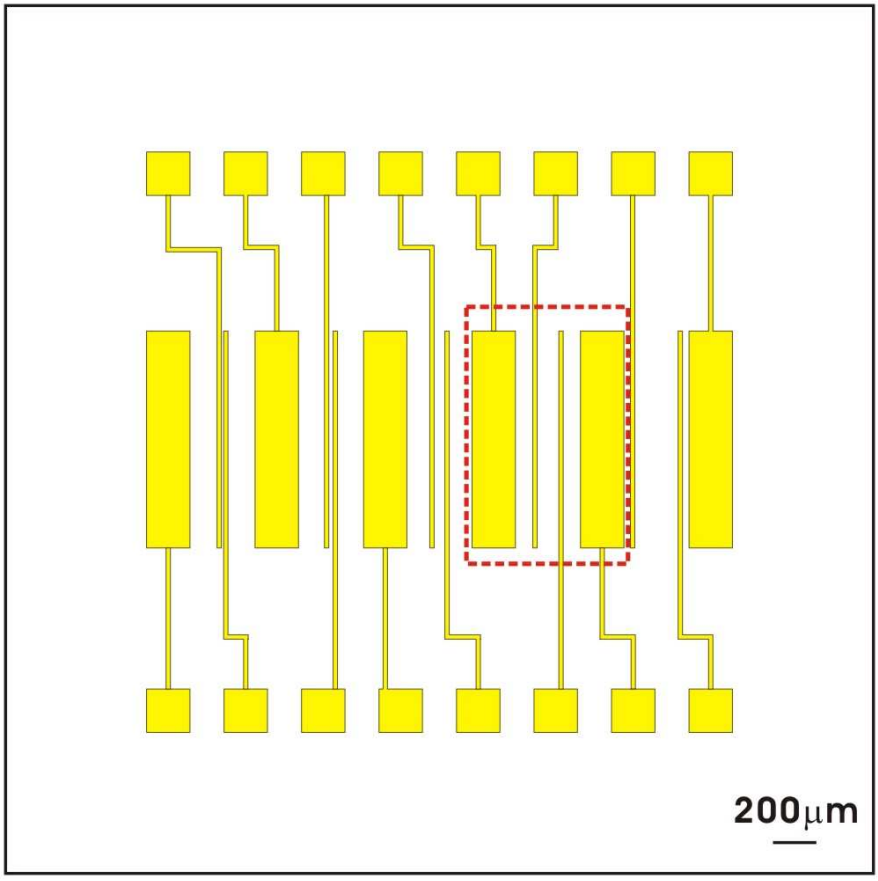


Figure 3.3: A typical leakage I-V characteristics when dielectric breakdown occurs.

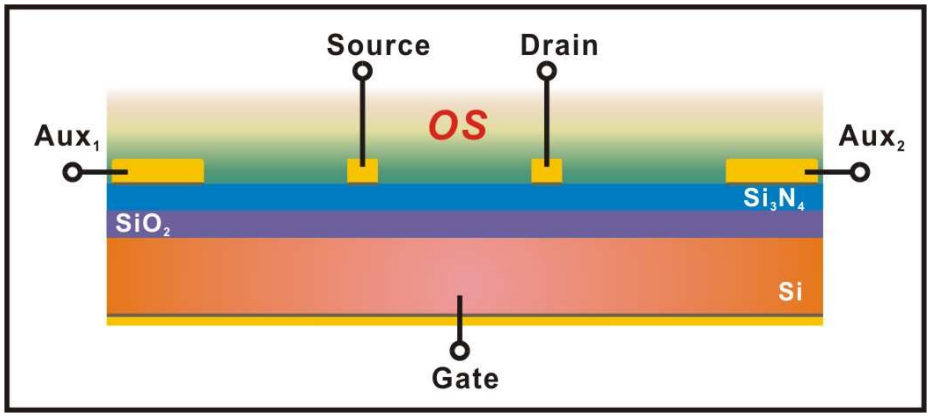
Before any measurements were taken, each IDS chip had to pass the leakage test consisting of grounding the top metallization and scanning the gate voltage applied across the chip in the range 0 and -80V. At the slow scan rate the correctly functioning chip should have only the capacitive charging current, below 100 pA level. When dielectric breakdown leakage occurs the leakage current exceeds 100 nA depending on the OS material. Such leakage current is a highly non-linear and irreproducible function of applied gate voltage (Fig 3.3). Obviously, once the chip has been compromised (i.e. leaked) it cannot be used for any meaningful tests and is discarded. The breakdown threshold level depends on the quality of the dielectric. In our chips the maximum "safe" gate voltage was -80V corresponding to the estimated field strength in the dielectric $\sim 10^7$ V cm^{-1}.

3.3 Four-point-probe measurements

Fig 3.4 shows the diagram of the top and of the side view of the individual IDS chip. The red dash line in Fig 3.4(a) defines a single 4-point-probe measurement unit. There is five such units in each IDS chip. In each unit, the center two thin electrodes can be viewed as the drain and source contacts for a "bottom contact" type organic field-effect transistors. The length of the channel is defined by the spacing of the drain/source electrodes (from edge to edge). They are 10 μm, 20 μm, 50 μm, 100 μm, to 200 μm, respectively. The width of the drain/source contact lines is 20 μm. The two outside thick electrode are independent current feeding auxiliary electrodes (Aux1 and Aux2), which are 200 μm wide and 1 mm long. The surface area of these auxiliary electrodes is purposely ten times larger than the surface area of the drain/source electrodes in order to facilitate impedance analysis of the contacts (not included in this thesis). The spacing between auxiliary electrodes is 300 μm. Thus, in this layout the chip has five independent four-point-probe units with



(a)



(b)

Figure 3.4: Diagrams of an interdigitated structure(IDS) chip. (a) top view of the test platform (in scale), red dash line indicates one 4-point-probe measurement unit with gate length = 100 μm (b) side view of an individual 4-point-probe measurement unit on chip.

variable spacing between the D and S electrodes, in 2-terminal or 4-terminal configuration. In this thesis, only the results of tests with 100 μm channel length devices are reported. The dependence on channel length will be discussed in future work separately.

In the 4-point-probe measurements the outer auxiliary electrodes are used for injection of variable current, which depends only on the applied auxiliary voltage and on the overall resistance between auxiliary electrodes. The inner measuring electrodes are designated "virtual source" (S) and "virtual drain" (D) because current does not flow through these two electrodes but the voltage drop can be measured through them, if we plot drain source current I_D versus voltage drop between the two electrodes V_{DS}, we can have a $I_D - V_D$ relationship of a "virtual OFET". In some tests described further they can be also used for injection of current.

3.4 Determination of resistance of the organic semiconductor

To determine the contact resistance of an OFET, a series of measurements have to be made with IDS. These tests are listed in the Table 3.1, it includes a 4-point-probe test, a 2-point-probe test, two 3-point-probe tests and leakage test, the connections, test parameters and results are also shown in the table.

The first set of measurements (Test I, Table 3.1) is performed in order to determine the true overall value of the device resistance.

$$R_{OFET} = R_{OS} + R_{Aux1} + R_{Aux2} \tag{3.6}$$

The device is shown in (Fig 3.4) is connected as follows: the current feeding electrode Aux1 is grounded and a voltage ramp (0 to -40V) is applied to Aux2 as shown in Fig 3.5(a).

Table 3.1: Summary of test protocols in determination of contact resistance of organic semiconductor

Test & figure	Connections	Measurements	Information
I - Fig 3.5(a)	Aux1, Aux2, S, D	$I_{Aux1,2}$ V_{DS}	R_{OS}
II - Fig 3.5(b)	S, D,	I_D, V_{DS}	$R_{OFET} = R_{OS} + R_S$
IV - Fig 3.5(c)	S, Aux2	$I_{Aux1,S}$, V_{DS}	$R_{OS} + R_S$
III - Fig 3.5(d)	Aux1, D	$I_{Aux1,D}$, V_{DS}	$R_{OS} + R_D$
V - Fig 3.3	Aux1, Au(back)	$I_{leakage}$	$R_{dielectric}$

The measurement is done for applied gate voltages V_G in the range (0 to -80 V). These measurements yield the conventional "$I_D - V_D$" characteristics of an OFET with the gate length of 300 μm as the black lines shown in Fig 3.6. In such measurements the film and the contact resistances are lumped together. Obviously, the carrier mobility calculated from such measurements is in error.

In the four-point probe measurements, virtual source S and virtual drain D leads are used to monitor the potential difference V_{DS} in the P3HT film. Test results yield the "virtual" I_D-V_{DS} characteristics for the "virtual Field-Effect Transistor" with a gate defined by the separation of the contacts S and D. In this "virtual FET" case, the I_D current doesn't pass through the metal/OS interfaces at S and D, and there is no contact components included in the experimental values of the "virtual" I_D-V_{DS} characteristics. By dividing V_{DS} by I_D, we can obtain the resistance value R_{OS} of the OS film located between S and D electrodes for different values of applied voltage V_G and from that calculate the carrier mobility equations 3.1, 3.4.

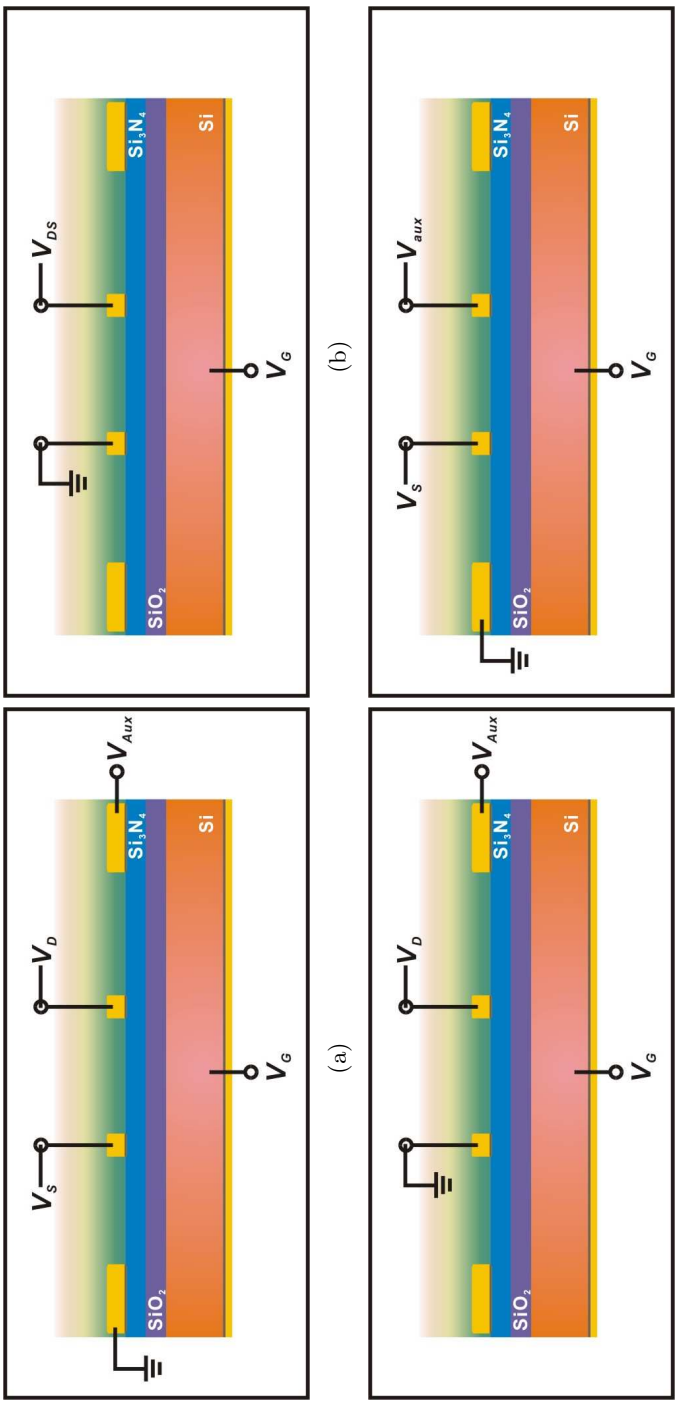


Figure 3.5: Connections for contact resistance measurements. (a) 4-Point-Probe Measurement for R_{OS} (b) 2-Point-Probe measurement for R_{OFET} (c) 3-Point-Probe measurement for $R_{OS} + R_S$ (d) 3-Point-Probe measurement for $R_{OS} + R_D$.

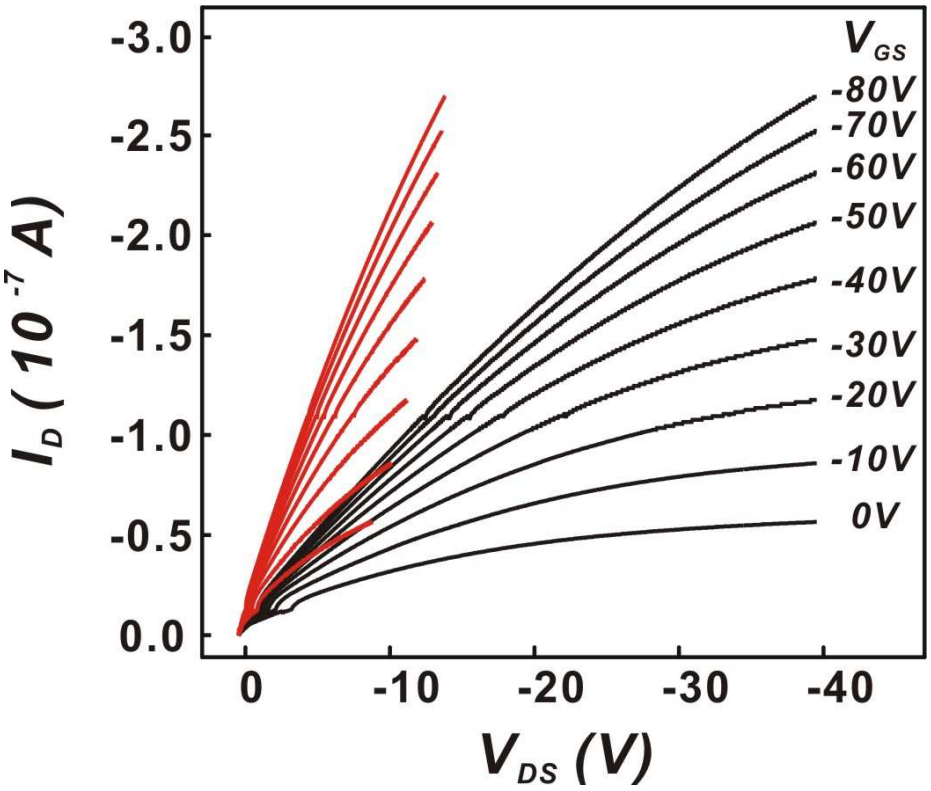


Figure 3.6: $I_D - V_{DS}$ characteristics of a "true" OFET (black lines) and a "virtual" OFET (red lines). Aux1 was grounded and voltage (0 to -40 V) was applied at Aux2, gate voltage is in the range (0 to -80 V). The channel length of the true OFET is L= 300 μm and the channel length of the "virtual" OFET is L=100 μm. In "virtual OFET" the V_{DS} corresponds to the potential difference recorded at S and D electrodes.

3.5 Determination of contact resistance

In this experiment (Test II), the source lead S is grounded and the voltage V_{DS} is applied to the drain lead D. In this case, the gate length is 100 μm, However, since the current passes through both metal/OS interfaces at S and D, this measurement includes both the source resistance R_S and the drain resistance R_D, as well as the film resistance R_{OS}. From the ratio of V_{DS} / I_D, the overall resistance of the OFET is obtained.

$$R_{OFET} = R_{OS} + R_S + R_D \tag{3.7}$$

The I_D-V_{DS} characteristics of this measurement with the P3HT as organic semiconductor are shown in Fig 3.7(a). This again is the commonly reported characteristic for the OFET with 100 μm channel length.

In order to separate the contribution of the contact resistances at drain (D) and Source (S), two additional experiments are performed, the connections are shown in Fig 3.5(c) (d). First, the S is connected to ground and a voltage ramp is applied to the Aux1 electrode (Test III) while recording the voltage at the D electrode (note again that no current flows to D). Current is plotted vs. potential difference V_{DS} between source S and drain D. The result is shown in Fig 3.7(b). In the second experiment (Test IV) the source lead is grounded, the voltage is applied to Aux2, and the voltage at the D lead is recorded. The result is shown in Fig 3.7(c). From these measurements we obtain $R_{OS} + R_S$ and $R_{OS} + R_D$, respectively. Since the overall resistance R_{OFET} and OS resistance R_{OS} are already known eq 3.7, the drain contact resistance and the source contact resistance can be calculated. The sequence of experiments is summarized in Table 3.1 which lists all the tests that need to be made, together with the parameters from which the information is obtained.

3.6 Field modulation

The above measurements are made for the set of applied gate-source voltages V_G (0 $\sim$ -80 V). Thus, the effect of the applied gate field on individual resistances can be evaluated. The results are shown in Fig 3.8. There are two most striking observations. First, the magnitude of the field modulation of the drain contact resistance R_D and of the OS film resistance R_{OS} are comparable. In other words the observed overall OFET "field-effect", at least in this device, can be attributed equally to the drain contact and to the OS modulation by the gate field. The second notable observation is that the value of the source contact

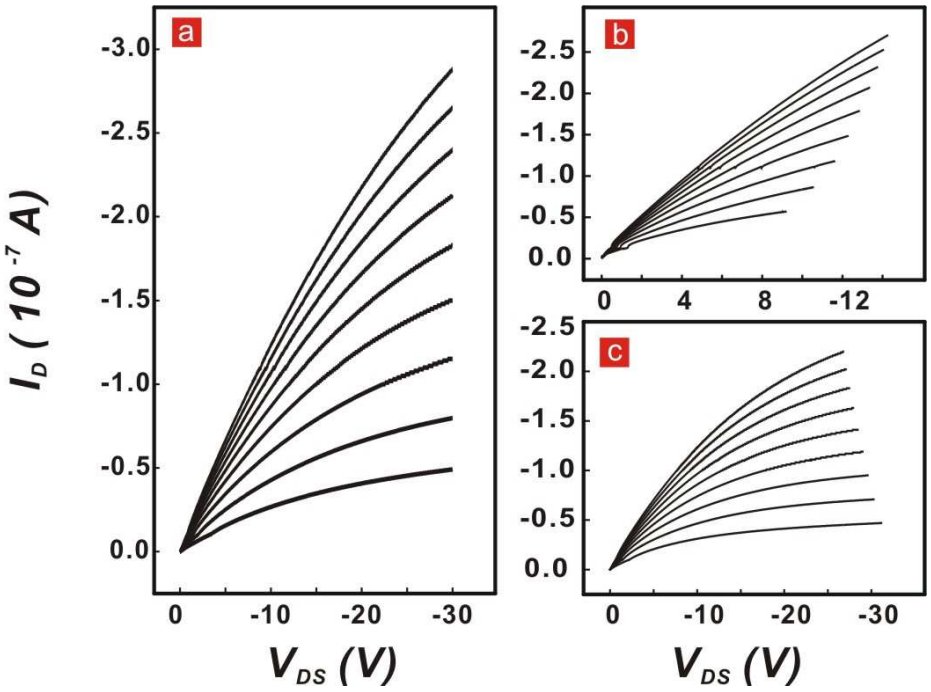


Figure 3.7: $I_D - V_{DS}$ characteristics of OFETs with L=100 μm. (a) Determination of R_{OFET}. Source (S) was grounded and voltage was applied at drain (D). (b) Determination of R_S. Source (S) was grounded and voltage was applied at Aux2. (c) Determination of R_D. Aux1 was grounded and voltage was applied at drain (D).

resistance R_S is small compared to the drain resistance. This observation agrees with the results obtained from the scanning Kelvin probe measurements.[121, 123, 124]

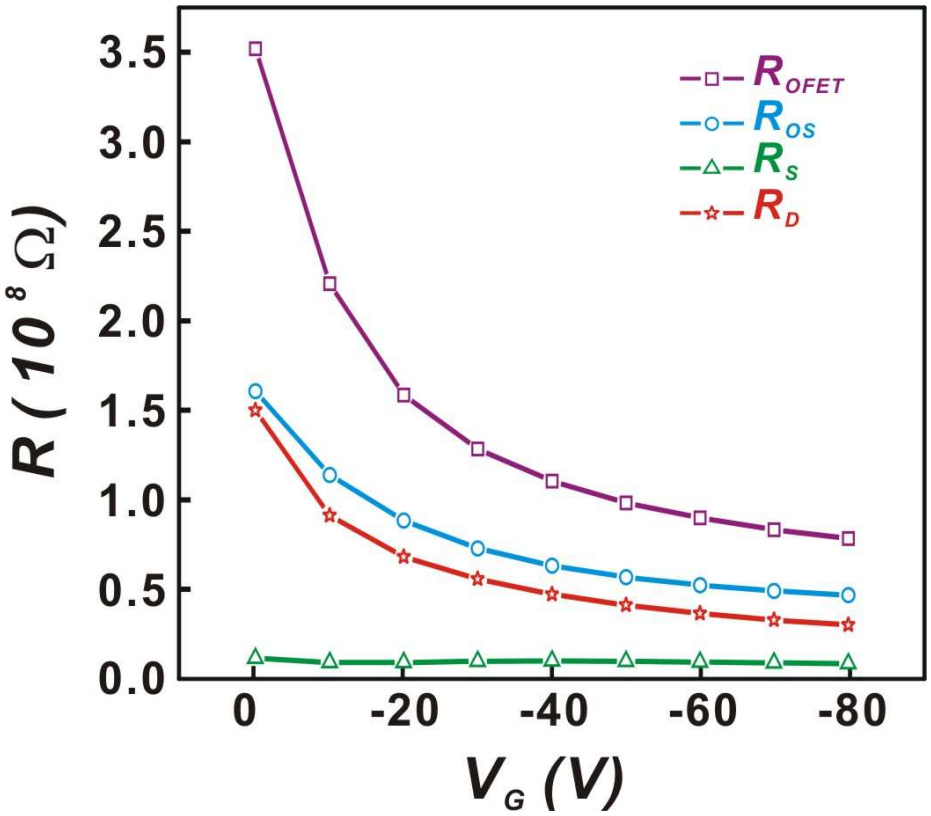


Figure 3.8: Modulation of the calculated (purple) overall OFET resistance R_{OFET}, (blue) organic semiconductor resistance R_{OS}, (red) source contact resistance R_S and (green) drain contact resistance R_D by applied gate voltage V_G.

The characteristics of a IGFET with gate capacitance C_0 are typically shown in form of current-voltage relationships given by equations 3.1, 3.4. And the channel transconductance g_D is then given as the slope of the $I_D - V_G$ curve in the linear region, for a give V_{DS}

$$g_D = \left(\frac{dI_D}{dV_G}\right)_{V_{DS}} = \frac{\mu C_0 W}{L}(V_G - V_T) \tag{3.8}$$

From this value the carrier mobility μ can be evaluated for a given V_G. Because carrier mobility is the material property, it must be extracted from the film resistance R_{OS}, rather

than from the overall resistance which includes the contact resistance. The current-gate voltage relationship in Fig 3.9 needed for this calculation is reconstructed from the four-point probe measurements described above. The drain contact resistance R_D has its origin in the formation of the space charge, which translates into effective contact resistance. Thus, when current passes through the channel even a perfectly ohmic contact develops depletion space charge and with it the corresponding field-dependent contact resistance. The current at metal/semiconductor junction can be described by the Mott-Gurney equation[79] which for planar junction is

$$J = \frac{9}{8}\mu\epsilon\frac{V^n}{d^3} \tag{3.9}$$

Where $n > 2$. The drain contact resistance can be then written as

$$\left(\frac{dV_{DS}}{dJ_D}\right)_{V_G} = R_D = \frac{8d^3}{9\mu\varepsilon n V^{n-1}} \tag{3.10}$$

In these equations d represents the thickness of the space charge, ϵ is the permittivity and μ is the charge carrier mobility. The electric fields that correspond to V/d are additive, which means that the electric field in the space charge, and thus the contact resistance, is affected by the combined effect of the V_{DS} and of the parallel component of the field due to V_G. Curves shown in Figure 6 are not the 8 typical I_D- V_G characteristics but just a small section of the I_D- V_G characteristics at the transition between linear (eq 3.1) and saturation (eq 3.4) regions.

The inverse contact resistance (conductance) and the drain current in the linear region are both linearly dependent on the applied gate voltage. This functional similarity often leads to confusion when the $I_D - V_G$ and $I_D - V_{DS}$ are superficially, visually examined

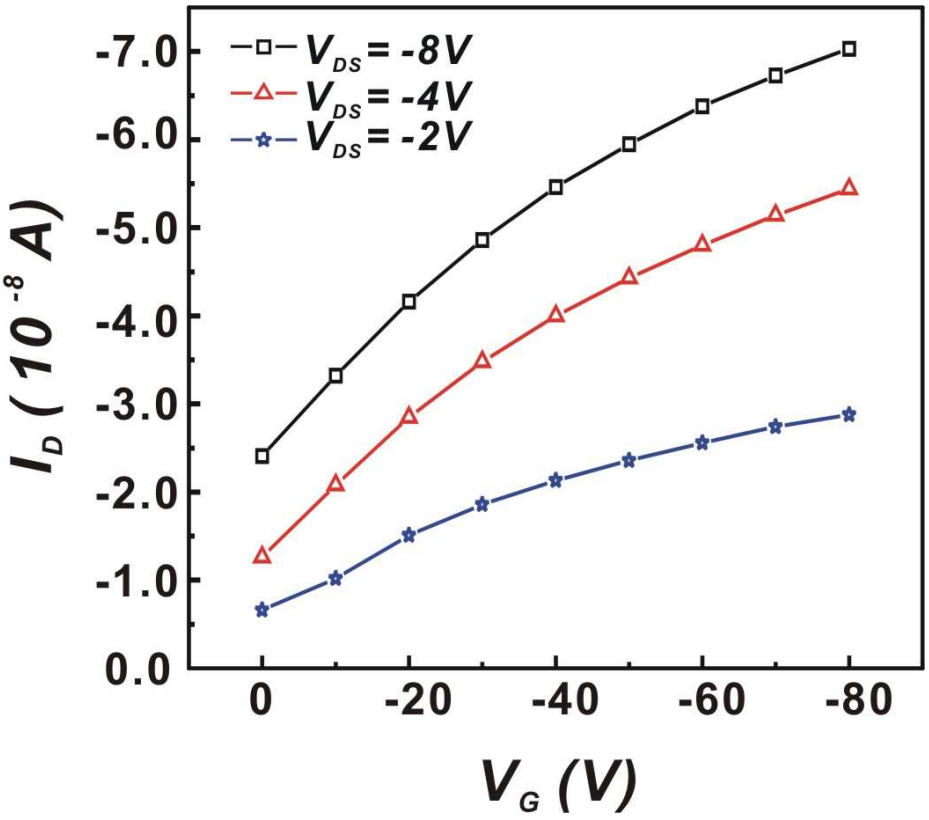


Figure 3.9: Corrected contact-free $I_D - V_G$ characteristics of an OFET with L=100 μm channel at three drain voltages, (black) V_{DS} = -8V (red) V_{DS} = -4V (blue) V_{DS} = -2V.

from the overall characteristics. The matter is even worse when the drain current is plotted on logarithmic scale because logarithmic function obscures the differences that would be otherwise apparent on a linear plot.

3.7 Conclusions

The main objective of this chapter has been to develop a methodology that would allow experimental separation of the field-modulation effects in co-planar OFETs. By "co-planar" we mean the device in which both the contacts and the channel are exposed to the same electric field. This is a different situation from that found in a conventional silicon-based insulated gate field-effect transistor where the contacts are deposited on top of the thick "field oxide" whose sole purpose is to remove them from the gate field.[94] Because interdigitated substrates are fabricated "inexpensively" in a "one-mask process" they are the most popular vehicles for the study of OFETs. In both the "bottom contact" and the "top contact" geometries the contacts and the interface between the OS and the dielectric are exposed to the electric field from the gate electrode. This study has indeed confirmed that both the drain contact and the bulk of the OS are indeed modulated by the gate field and that this modulation has similar functional relationship and magnitude. The contribution from the source contact modulation is relatively minor (Fig 3.7). In the schematic diagram of the device Fig 3.1(b) the electrodes are shown as "metal rectangles". In reality, the profile of the metal contacts depends on the deposition conditions and could be anything but rectangular. In that case the superposition of the electric fields contributed by the drain and by the gate voltages can be very complex and highly specific to the individual device. In other words the relative contribution of the two fields varies from one preparation to another. It is not surprising that under those conditions the variability of the reported

"carrier mobilities" obtained from uncorrected $I - V$ dependencies is very large.

A simple leakage test has been included in our test protocol Table 3.1. It helps to identify the presence of the parasitic leakage current that would otherwise corrupt the experimental data and its interpretation. Unfortunately, the presence of leakage current is seldom verified and almost never reported in the OFET literature despite the fact that results clearly show its presence.[125] A statement about the verification of integrity of the test platform should always be made particularly when the drain current does not pass through zero at the zero applied V_{DS}.

The OS used in this study, poly(3-hexylthiophene) is one of the more popular materials commonly used in OFETs. We have neither prepared nor evaluated the films under controlled conditions (i.e. dry nitrogen) because our objective has been the introduction of the method rather than a study of a material. Therefore we are not reporting any values of mobilities, that seem to be the holy grail of most OFET publications. The origin of the field-modulation of the resistance of the OS/dielectric interface is subject of much speculation.[123,126–131] The modulation of carrier mobility or charge carrier density, or both are possible.[124,132–137] Similarly, the origin of the modulation of R_{OS} at the molecular level is not clear.[138,139] It is our hope the IDS test structure may facilitate further research in this area and help to clarify some controversial results.

CHAPTER IV

OXYGEN DOPING IN POLY(3-HEXYLTHIOPHENE)-BASED ORGANIC FIELD-EFFECT TRANSISTORS

4.1 Introduction

From the discussion in chapter II, we already know that ambient environment can affect the properties of organic electronics from different aspects. For the poly(3-hexylthiophene) (P3HT) based OFET as we studied in the previous chapter, oxygen is a critical factor that affect its properties. In the previous study, we can see the P3HT OFET does not have a fully off state, as a result, the on/off ratio of this OFET is very poor (just about $2 \sim 3$). In this chapter, we show how to remove the influence of oxygen from P3HT OFET, and also we discuss how the oxygen doping affects the properties of P3HT OFET.

4.1.1 Oxygen doping on poly(3-hexylthiophene) organic field-effect transistor

It has already been demonstrated that when P3HT based OFET is processed in ambient conditions, it exhibited lower mobility and significantly lower current on/off ratio.[118] Most interference from ambient air comes from oxygen. Oxygen can form change transfer complex (CTC) with P3HT.[4] In this case, the π-conjugated polymer P3HT is an electron donor (D), and oxygen with high electron affinity is an electron acceptor (A). Electron donor and electron acceptor forms a weakly bound donor-acceptor complex or CTC as shown in equation 4.1. Upon association, the physical properties of the donor and acceptor are

perturbed and new properties arise.

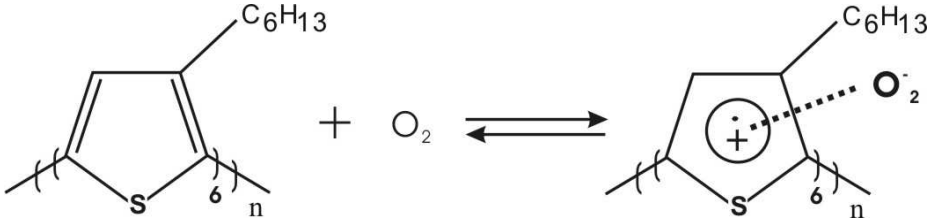


Figure 4.1: Schematic diagram of poly(3-hexylthiophene)-oxygen charge transfer couple complex formation from.[4]

$$D + A \rightleftharpoons [D^{\delta+} \cdot A^{\delta-}] \tag{4.1}$$

P3HT will undergo chain scission in organic solvents when irradiated with UV-vis light.[140] The quantum yield of chain scission depends on the presence or absence of oxygen, the nature of the solvent and wavelength of incident light. The formation of photochemical residues in the main chain reduces the number of π-electron conjugated sequences.

From the information above, we can see that the influence from oxygen will have two aspects. The formation of CTC will introduce more main charge carriers (holes) into the bulk of P3HT OFET, thus significantly increase the off state current, then reduce the on/off ratio of the device. On the other hand, the solvent residue in the OFET bulk will contribute to the degradation of P3HT film under UV-vis light, as a result, the polymer chain length is reduced, the charge transfer along the polymer chain will be reduced, then the OS conductivity decreases. So, the final effect from oxygen would be a combination of above two process. And the diffusion of oxygen in the OFET bulk also has to be considered in the real application. In this chapter, we will discuss these factors in detail.

4.1.2 Encapsulation of poly(3-hexylthiophene) organic field-effect transistor

Packaging process is very important in IC fabrication. It insulates the electronics from the ambient environment and helps to dissipate heat, and enhance the electronics performance.

In the organic field-effect transistor, packaging has not yet been widely used partly because OFET still can't not met the requirements for commercialization. Now, most of the research on P3HT based OFET is performed in glove box under the protection of inert gas. For the real application, the OFET has to be stable in ambient air. To reach this goal, encapsulation is a necessity .

There are several requirements for the encapsulation materials. They should be soluble so that they can be spin cast onto device, they also need to be solvent resistant after curing or cross-linking. They should be photo-patternable, so it can be made into desired pattern. Other requirements include chemical inertness, electrical passivating, moisture and oxygen resistant, and good adhesion to the device surface.

Oxygen barrier material Poly(2-allyl,6-methyl-oxyphenylene)(PAMOP)[141] has been tested in this thesis for encapsulation purpose. Its strucure is show in Fig 4.2. It was synthesized in Institute für Mikrotechnik Mainz GmbH, Germany. PAMOP is a derivative of poly-oxyphenylene, which is known to be chemical resistant and shows a good adhesion to silicon oxide surface. PAMOP is synthesized in a low molecular weight precursor where each phenylene unit comprises a thermal cross-linkable functional group (allyl), and a methyl group in 6 position which helps to reduce the curing temperature. The low molecular weight precursor is soluble in common solvents (e.g. methylisobutylketone(MIBK), cyclopentanone, tetrahydrofuran (THF), chloroform, dimethylformamide (DMF), methanol, etc.). After curing at

120 ∼ 150 °C for at least 30 min, the highly cross-linked (in this case 100% cross-linked) PAMOP is not soluble. The barrier properties of PAMOP are dependent on the diffusion or the permeation of gas molecules through the film, and this can be controlled by the cross-linking degree. In this chapter, PAMOP is used as P3HT encapsulation layer. Test results show some attractive features about this material.

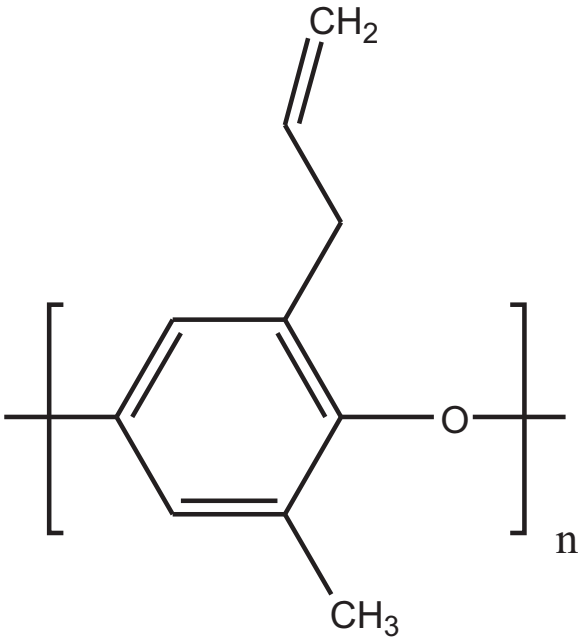


Figure 4.2: Schematic diagram of chemical structure of Poly(2-allyl,6-methyl-oxyphenylene) (PAMOP) repeating unit

4.2 Experimental

The fabrication process of interdigitated structure (IDS) has been described in chapter III. IDS chip is attached to a 28 pin DIP ceramic header (Edison Engineering Inc.) using silver based conducting epoxy, it is bonded to the header with gold wire.

IDS chip is sonicated in isopropanol for 2 min, rinsed with DI water, and then blow dried with nitrogen. After that, the chip is cleaned with oxygen plasma for 5 min to remove any organic residue. Cleaned IDS chip is then spin coated with a thin layer of HMDS

(hexamethyldisilazane). The spin speed is 2000 rpm, for 30 sec.

Regio-regular poly(3-hexylthiophene) (P3HT) is used as received without further purification. P3HT is dissolved in chlorobenzene, the typical concentration is 1 mg/mL. P3HT solution is drop cast on the IDS surface with a 10 μL syringe. The chip is then put in the vacuum desiccator to remove solvent residue, and then placed in the vacuum oven at 150 °C for at least 30 min to remove trapped oxygen. During the process, the OFET is kept in dark. The thickness is in the range of 50 $\sim$ 400 nm.

PAMOP comes in the form of oligomer precursors. PAMOP is dissolved in THF, the typical concentration is about 20 mg/mL. The PAMOP solution is then drop cast on top of the P3HT film. After that, the chip is placed in the vacuum oven at 150 °C for about 1 hour to cross-link the PAMOP precursor. The thickness of the PAMOP encapsulation layer is in the range of 200 $\sim$ 600 nm. Film thickness was measured with Dektak 3_{ST} profilometer

Electrical measurements were performed with HP 4155A parameter analyzer equipped with 16442A test fixture. Leakage test described in chapter III were performed each time before starting any other tests. The instrument has a input bias current about 10 pA, so in all tests, two differential amplifiers with ultra-high input impedance ($> 10^{15}\Omega$) were added as unity gain buffers.

4.3 Oxygen doping removal by annealing method

The charge transfer couple formed between P3HT and oxygen is a weakly bound complex, the equilibrium constant calculated is about 0.47 M^{-1} based on the equation 4.2. It means that this CTC can be easily broken down under certain conditions, such as heating. Actually this procedure has been used to removed the influence from oxygen.[142] In our experiments, it has been found that by annealing the P3HT OFET in vacuum oven at 150

°C for 30 min to 1 hour will remove the influence from oxygen. The test results are shown in Fig 4.3

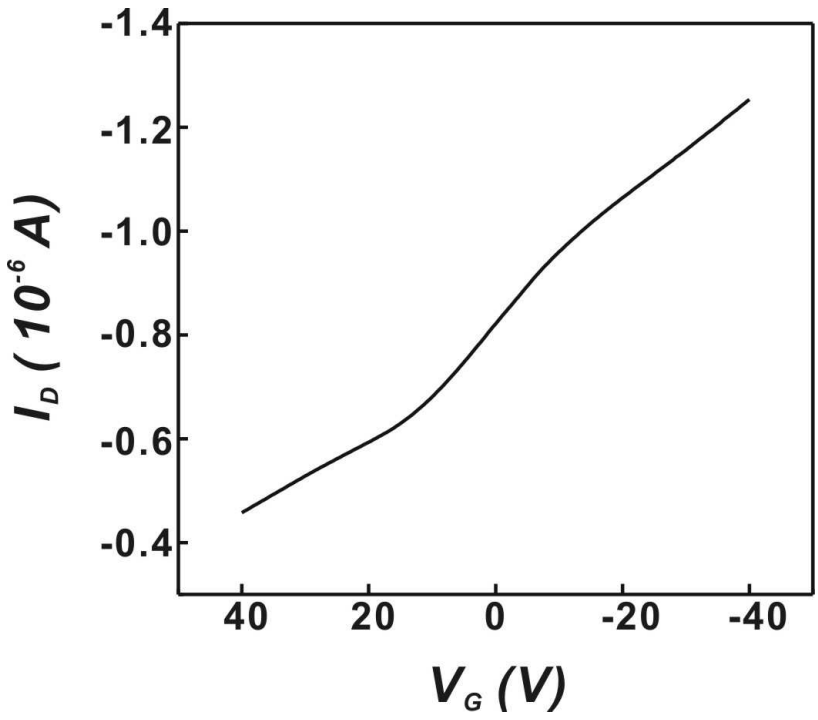
$$K_c = \frac{[CTC]}{([D] - [CTC])([A] - [CTC])} \tag{4.2}$$

In Fig 4.3(a), P3HT was just cast and dried on IDS structure, since the P3HT solution is already saturated with oxygen, we can see the on/off ratio is only around 3, and because there is no actual off state, it is hard to find out the threshold voltage for this device. After 1 hour annealing process, we got the test result shown in Fig 4.4(b). This results shows an on/off ratio of $\geq 10^3$, the off state current is reduced to 10 pA level which is almost the instrumental limitation. The charge carrier mobility calculated from the curve is $3.76 \times 10^{-5}\ cm^2/Vs$. This test shows that annealing is an effective method of removing oxygen influence.

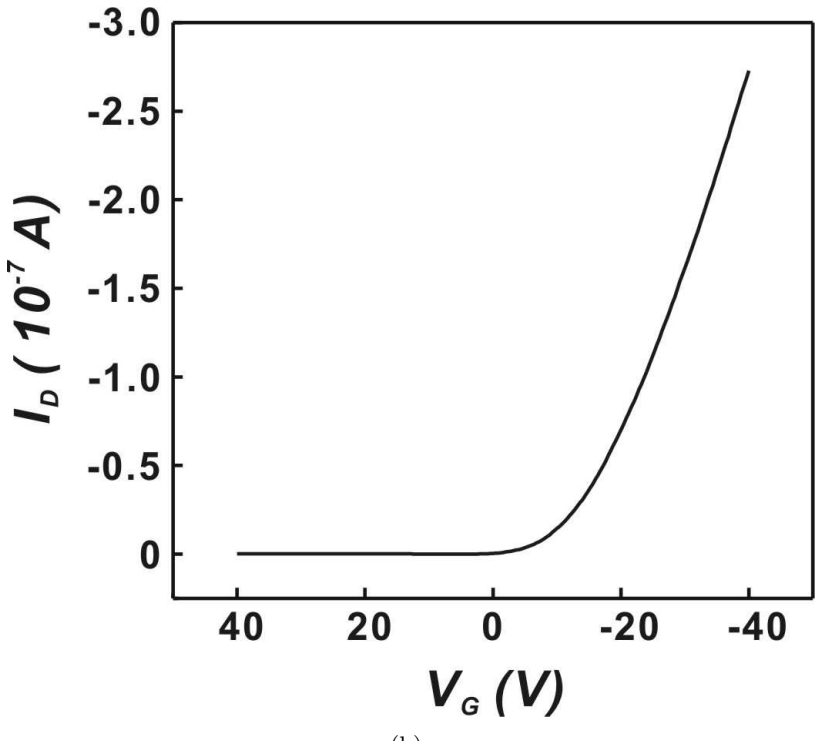
In Fig 4.4(a), the P3HT OFET is measured just after the annealing process, Fig 4.3(b) is measured after 1 hour staying in ambient air. We can see the rapid increase of the off state current, which shows that the formation of CTC is very fast. Also from Fig 4.3 and Fig 4.4 we can see that the formation of CTC is reversible.

4.4 Contact resistance in poly(3-hexylthiophene) organic field-effect transistor

The annealing procedure allows us to measure the characteristics of P3HT OFET without the interference from oxygen. With the systematic protocol suggested in chapter III, we can separate the contact resistance in our measurements. Fig 4.5 shows the contact resistances as the functions of gate electric field. This test confirms the results reported in chapter III. Another interesting observation is that under high positive gate voltage where

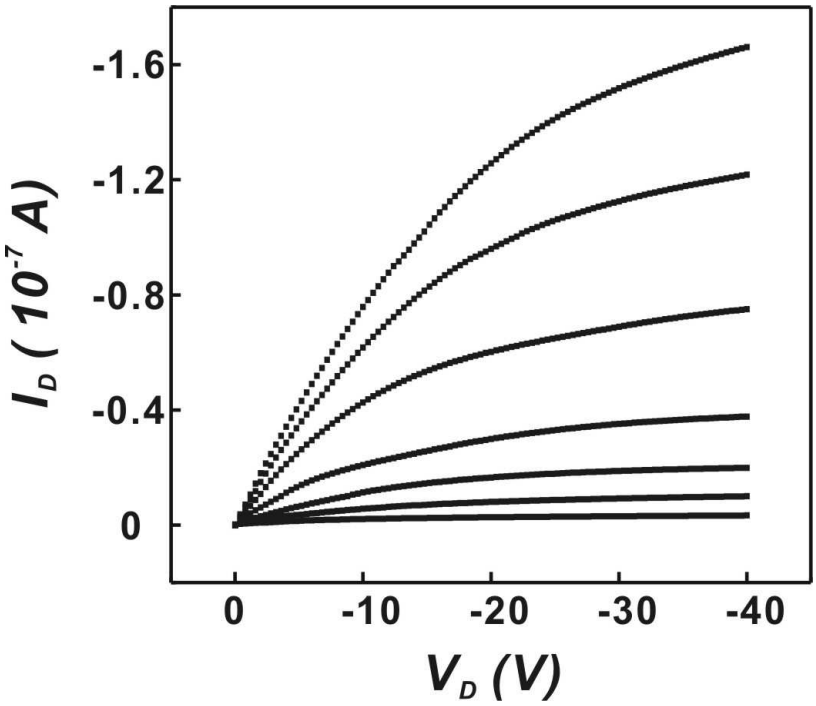


(a)

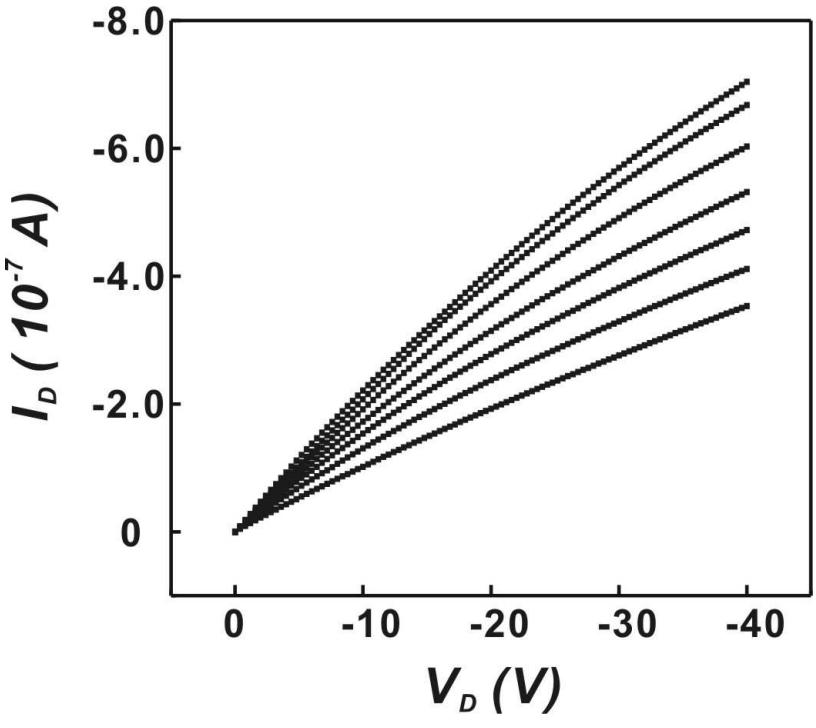


(b)

Figure 4.3: $I_D - V_D$ characteristics of P3HT OFET (a) before annealing ON/OFF ratio $\simeq 3$ (b) after annealing ON/OFF ratio $\geq 10^3$. V_D = -60V . Annealing is done by baking P3HT OFET in vacuum oven at 150 °C for 1hr.



(a)



(b)

Figure 4.4: $I_D - V_D$ characteristics of P3HT OFET (a) immediately after annealing (b) 1 hour after annealing. V_G = 30V to -30V, step is -10V. Annealing is done by baking P3HT OFET in vacuum oven at 150 °C for 1hr.

the OFET is in the off state, the drain contact resistance R_D is dominant, as the gate voltage becomes more negative, its value rapidly decreases and it becomes the minor component in the OFET. This fact shows that in the real application, contact resistance is actually beneficial. At high positive gate field, big contact resistance helps the OFET to stay in off state, and at negative gate field, this contact resistance decrease faster than OS bulk resistance, then becomes less important.

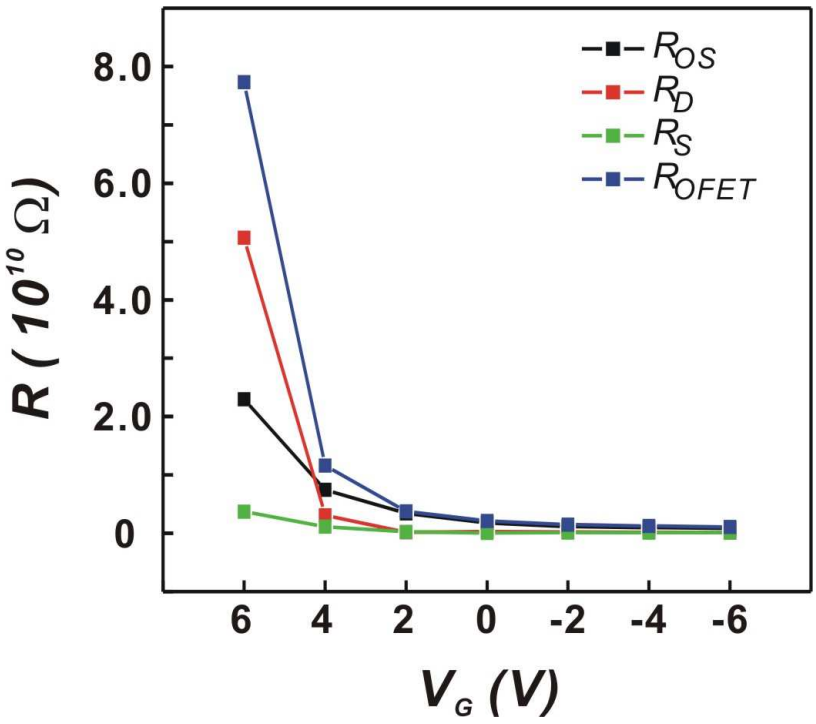


Figure 4.5: Film resistance R_{OS}, drain contact resistance R_D, source resistance R_S and total resistance R_{OFET}as functions of gate voltage (V_G) change. V_D = -1V.

4.5 Contact free $I_D - V_G$ characteristics of P3HT OFET

Fig 4.6 shows the contact free $I_D - V_G$ characteristics of P3HT OFET, in this test, the $I_D - V_G$ characteristics has been corrected by performing 4-point-probe measurement which is outlined in chapter III. Unlike the curve shown in chapter III, in this figure, it clear shows that there exits the off state. From this figure, we can calculate the true charge

carrier mobility using equation 3.1. The calculated mobility is $1.65 \times 10^{-5}\ cm^2/Vs$.

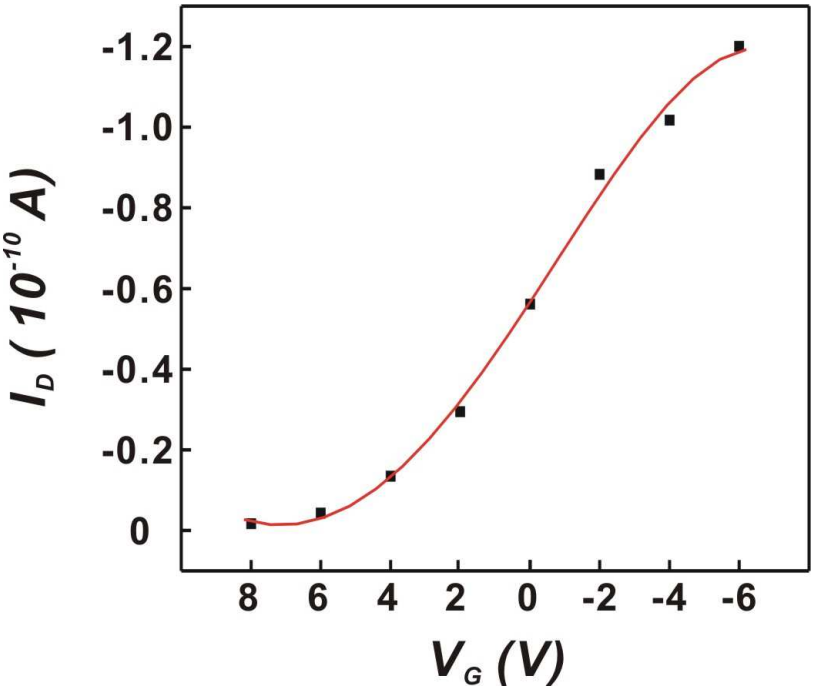


Figure 4.6: Contact free $I_D - V_G$ characteristics of annealed P3HT OFET, V_D = -1V.

Compared with the typical reported mobility value (0.1 cm^2/Vs for regioregular P3HT),[117] the mobility value we observed is very small. It is significant that this value is the true material property. It does not contain the influence from contact resistance at organic semiconductor/metal interface. Mobilities calculated directly from the conventional 2-point-probe are always affected by contact components. In chapter III, we demonstrated that the contact resistance is modulated by the gate electric field in a "co-planar" structure. If the calculation of charge carrier mobility includes the contact resistance components, we would expect that mobility value would be gate field dependant, and this has already been reported.[136] Charge carrier mobility is a material property, it depends on the chemical structure of the material and the doping conditions. Our approach allows to obtain "true mobility values" that do not include the contribution from contact resistance.

4.6 Oxygen doping effects on properties on poly(3-hexylthiophene) organic field-effect transistor

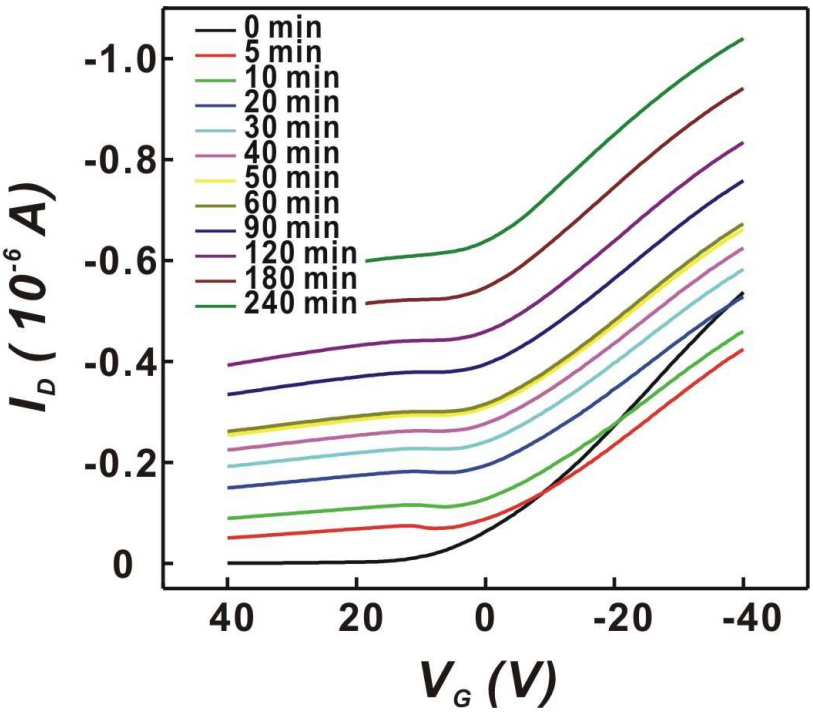
A series of tests have been made to test the functionality of PAMOP as the encapsulating layer for P3HT OFETs. The test results are shown in Fig 4.7 and 4.8. From the figure we can see that, first, PAMOP layer as the oxygen barrier can effectively slow down the oxygen doping speed, second, light plays a very important role in oxygen doping in P3HT OFETs.

4.6.1 Shifting of threshold voltage

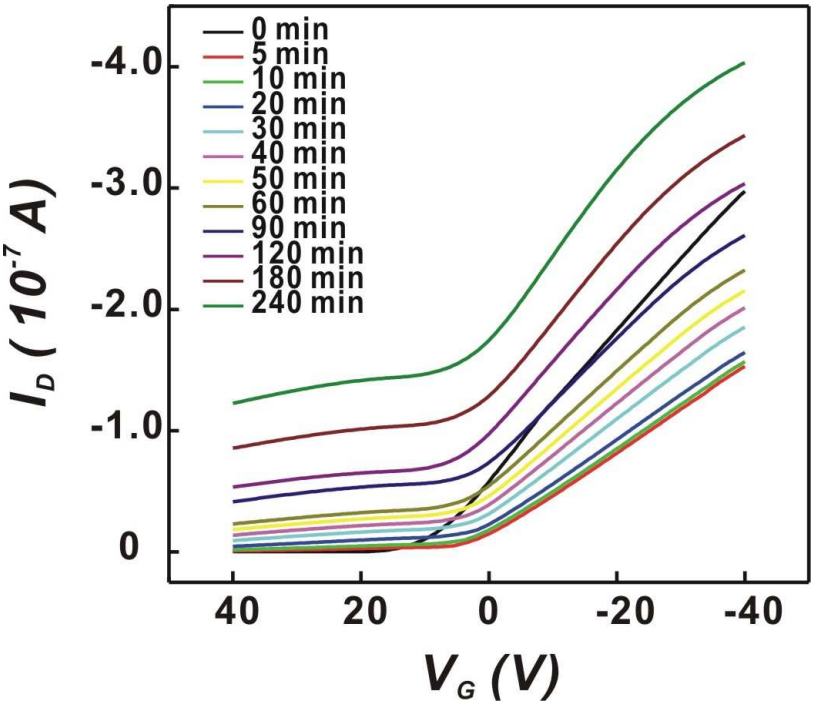
Even though PAMOP encapsulation layer can effectively slow down the oxygen doping, long-term test shows that this material still needs improvement. Fig 4.9 shows the P3HT OFET $I_D - V_G$ characteristics changes over 10 days. These measurements were performed using 2-point-probe configuration, so the change of contact resistance is also included in the results. It is clear that besides the decrease in on/off ratio (Fig 4.10), there is a shift of the apparent turn-on voltage V_T of this OFET in Fig 4.11, it is surprising to see that the shift of the apparent turn-on voltage is almost 7V over the time. According to the equation 3.2 on page 63, the change in WF and change in free carrier concentration (n_0) all contributes to the shift of V_T. As oxygen slowly permeates through the barrier layer, it forms the CTC with P3HT, thus changes the WF of P3HT. The formation of CTC results in more charge carriers (holes) in the bulk. In p-type OS, the increase in n_0 makes the V_T move to positive direction, the magnitude is related to the concentration of CTC in OS bulk.

4.6.2 Prototype model for oxygen doping in organic field-effect transistor

Upon oxygen doping, the contact resistance in OFET is expected to change. We performed the 2-point-probe and 4-point-probe measurements after the PAMOP encapsulated

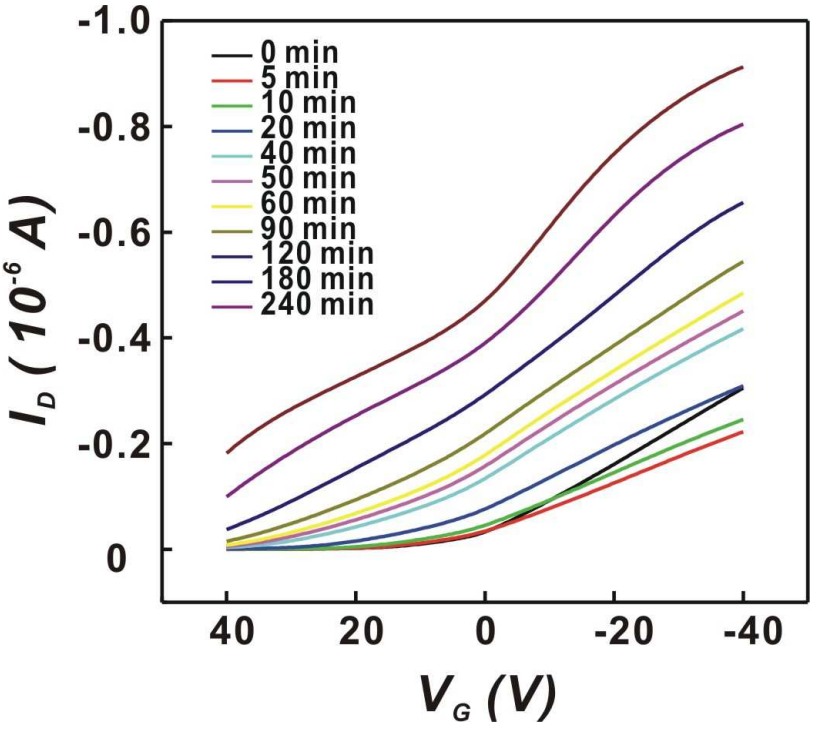


(a)

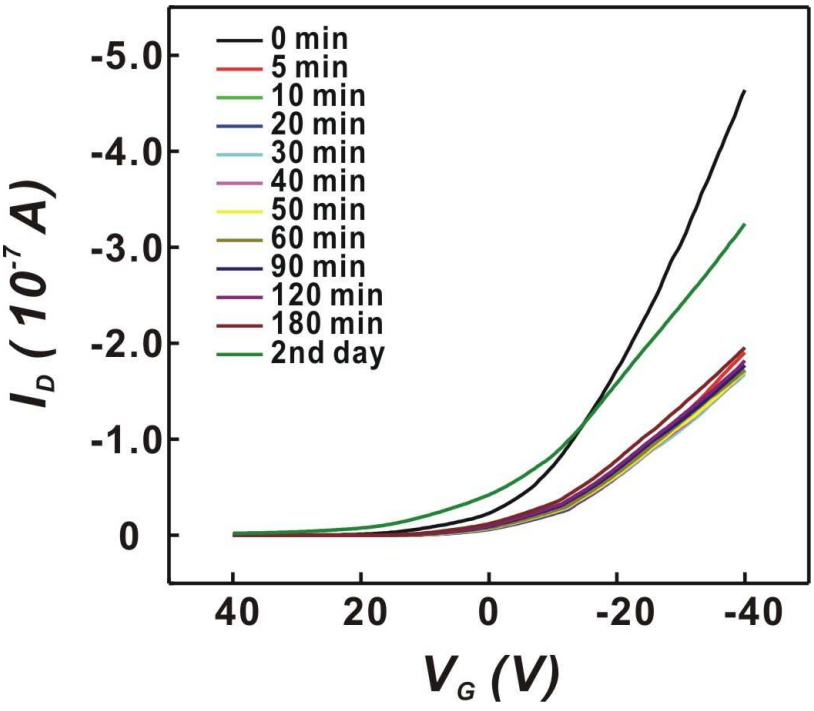


(b)

Figure 4.7: Influence of oxygen doping on $I_D - V_G$ characteristics of P3HT OFET without PAMOP encapsulation V_D = -60V (a) under indoor light (b) in dark.



(a)



(b)

Figure 4.8: Influence of oxygen doping on $I_D - V_G$ characteristics of P3HT OFET with PAMOP encapsulation V_D = -60V (a) under indoor light (b) in dark.

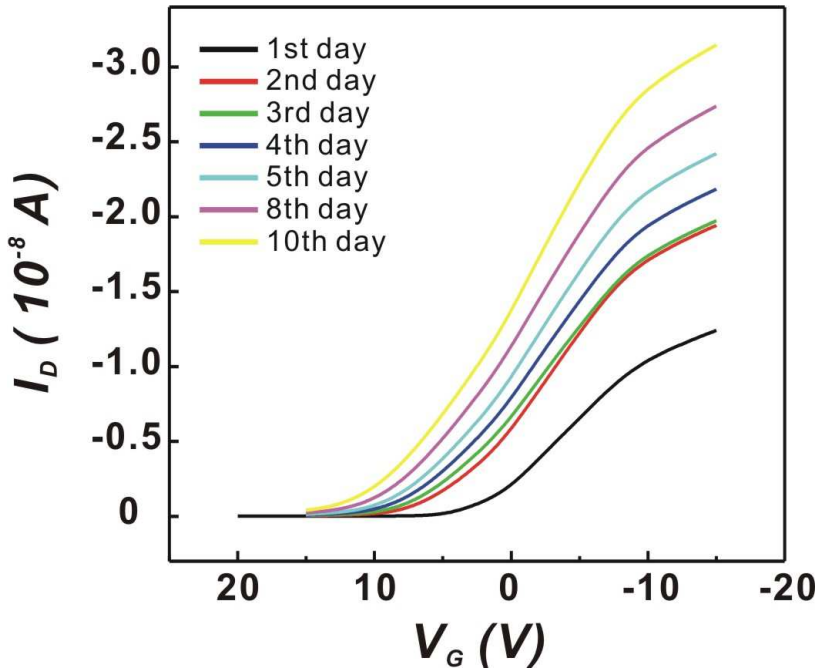


Figure 4.9: $I_D - V_G$ characteristics changes of P3HT OFET as function of oxygen doping time with the PAMOP encapsulation layer, V_D = -10V.

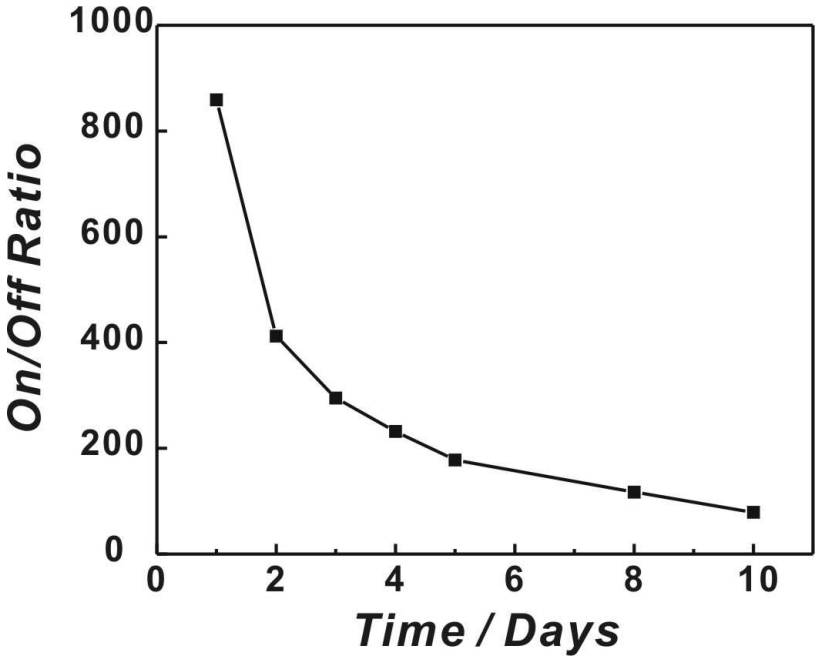


Figure 4.10: On/Off ratio changes of P3HT OFET as function of oxygen doping time with the PAMOP encapsulation protection. I_D at V_G = 15V is used as "off" state current, I_D at V_G = -15V is used as "on" state current.

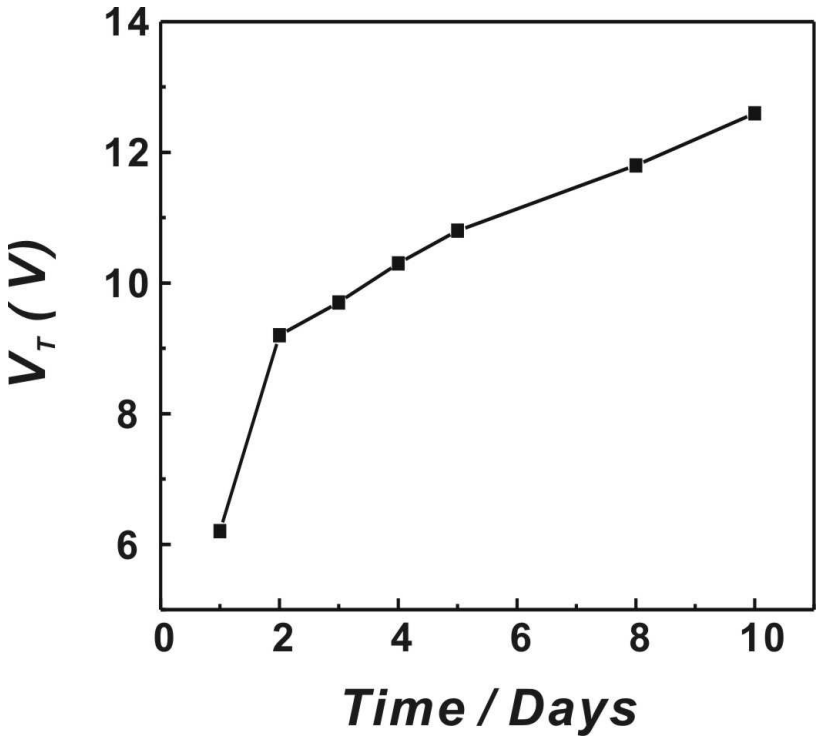


Figure 4.11: V_T changes of P3HT OFET as function of oxygen doping time with the PAMOP encapsulation protection, the value of V_T has been corrected to offset the influence from bulk resistance.

P3HT OFET was stored in dark for over 15 days. These two measurements show a apparent contradictory results: R_{OFET} value calculated from 2-point-probe measurement is lower than the R_{OS} value calculated from the 4-point-probe measurement. This indicates that new model has to be made to describe this situation.

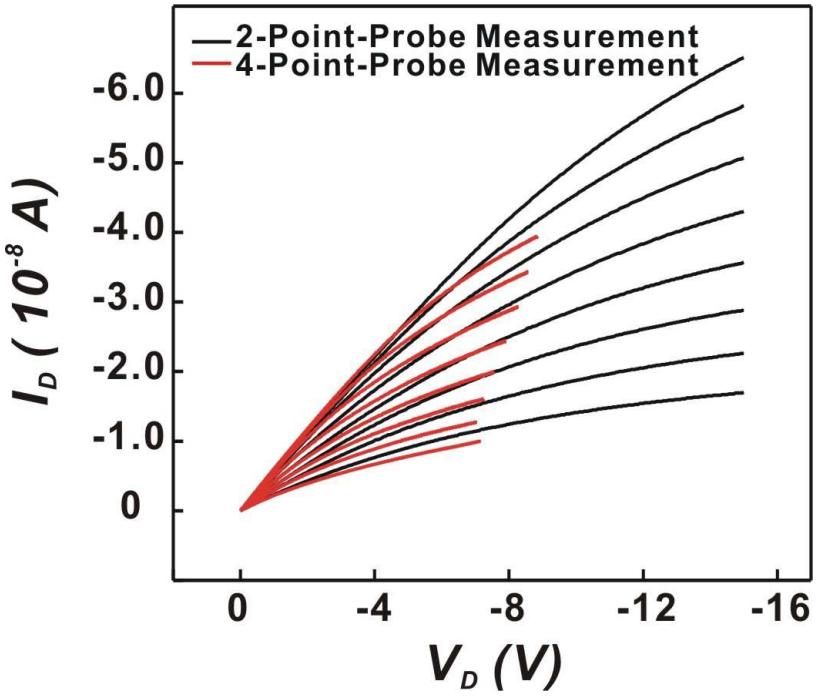


Figure 4.12: $I_D - V_D$ characteristics of P3HT OFET with L = 100 μm, V_G in the range of (8 $\sim$ -6V), step = -2V. (red lines) Measurements with 4-point-probe configuration. (black lines) Measurements with 2-point-probe configuration.

It has been demonstrated that all the charge of conducting channel resides in the layers next to the insulator-semiconductor interface.[143] In other words, OFET is modelled as a two-dimensional device. We can assume that the OS film can be divided into two layers: the bulk layer and the interfacial layer. The interfacial layer is under the modulation of gate field, while the bulk is unaffected by the gate field. Upon oxygen doping, there is a non-uniform distribution of oxygen present in the whole OS film, which affects both the interfacial layer and the bulk layer, the bulk layer which is closer to the top surface is

expected to have higher concentration of oxygen doping level, thus is expected to be more conductive than the interfacial layer. The equivalent circuit diagram is shown in Fig 4.13.

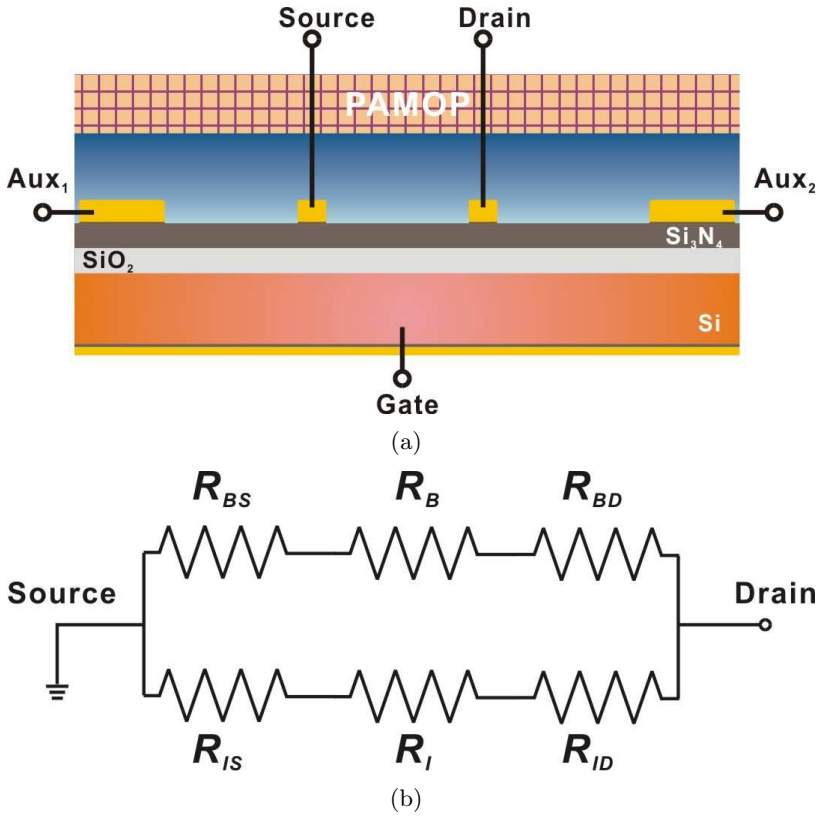


Figure 4.13: Schematic diagrams of equivalent circuit of P3HT OFET with PAMOP encapsulation layer when the organic semiconductor is partially doped with oxygen. (a) Schematic diagram of P3HT OFET with PAMOP encapsulation layer, side view. (b) equivalent circuit diagram for 2-point-probe measurement. R_{BD}, R_{BS} is the bulk layer contact resistance at drain and source, R_B is the bulk OS resistance, R_{ID} and R_{IS} are the interfacial layer contact resistance at drain and source, R_I is the interfacial layer OS resistance.

In the previous measurement, the P3HT film was either freshly casted or measured just after annealing step, so that the whole film was uniform, and the bulk resistance was never lower than the interfacial resistance. Under the situation, the previously suggested protocol works well. However in the oxygen doping case, bulk layer is more conductive, so that most current passes through the bulk layer rather than through the interfacial layer. The calculated value of R_{OFET} made from 2-point-probe measurements then becomes apparent

smaller because of the parasitic parallel current pathway through the bulk.

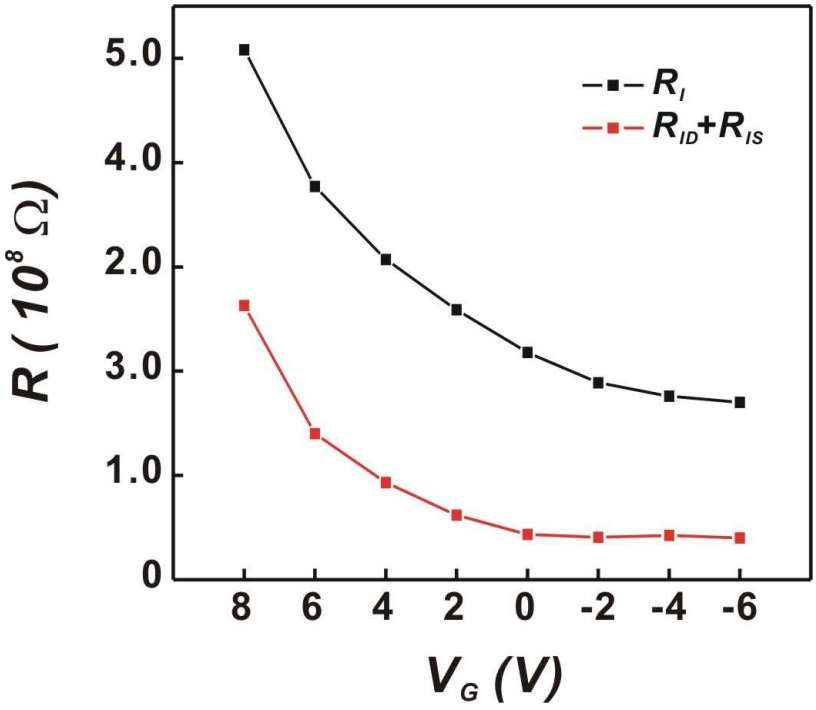


Figure 4.14: Modulation of calculated resistances as functions of gate electric field V_G. (red line) The summation of interfacial source contact resistance R_{IS} and interfacial drain contact resistance R_{ID}, (black line) interfacial OS resistance R_I.

It is possible to make an assumption that in the off state, the interfacial layer becomes so resistive that all the current passes through the bulk layer. In fact, that is the real situation in OFET. Under the off state, the $I-V$ curve made from 2-point-probe measurement can be used to calculate the bulk resistance value ($R_{BS}+R_{BD}+R_B$), and then to take this value as the constant bulk resistance value. From this measurement we can calculate the overall interfacial resistance value ($R_{IS}+R_{ID}+R_I$). The results are shown in Fig 4.14. The interfacial contact resistance from drain and source can be calculated as a whole, but they are not separable with this test protocol. However compared with drain contact resistance, the source contact resistance is very small and can always be neglected. So we can assume $R_{IS}+R_{ID} \doteq R_{ID}$, then use this data to make comparison with the previous test results.

Upon oxygen doping, both the interfacial OS resistance and the contact resistance decreased significantly, and they have similar change pattern versus the gate electric field. These test results demonstrate that the oxygen doping in P3HT OFET can change all the resistance components in the model (Fig 4.13). Because of this interference, new method has to be developed to separate the interfacial drain and source contact resistances.

4.7 Conclusions

Oxygen is the most common interferer for most π-conjugated organic semiconductor materials. It forms weakly bond charge transfer complex with π-conjugated polymers and changes their properties. For P3HT based OFET, oxygen doping can increase the off state current and shift the turn-on voltage. By annealing process, oxygen can be removed from the OFET and its properties can be recovered.

PAMOP has been demonstrated to be an effective encapsulation material for P3HT OFET over short time period. By using PAMOP encapsulation, a non-uniform oxygen distribution has been created in OFET film, this results in creation of parasitic pathway of current in P3HT bulk. A model has been built to explain the test results. It is demonstrated that the oxygen doping can change both the bulk resistance and the contact resistance significantly.

CHAPTER V

FUTURE WORK

5.1 Investigation of the influence of channel length on organic field-effect properties

In field-effect transistors, channel length (L) is a very important parameter. It decides the geometry of the transistor. As the growth of modern technique, the requirement on the channel length becomes more and more critical. The very large scale integration requires the basic units - transistor to be smaller and smaller. As the channel length is reduced, the behavior of FETs departures from long-channel behavior, it is called the short-channel effect,[39] it arises as the result of a two-dimensional potential distribution and high electric field in the channel region.

In the short-channel situation, as the electric field increased, the channel mobility becomes field-dependent, and eventually velocity saturation occurs.[39] If further increases the field, carrier depletion near the drain occurs, and it can also cause hot-carrier injection into the oxide, leading to oxide charging and subsequent threshold voltage shift and transconductance degradation.

Same situation happens to organic field-effect transistor also. Even though not much focus has been put on decrease the OFET size, we can foresee it in the near future when new materials come out which meet the industrial requirements. It is necessary to know the influence of channel length on behavior of OFETs. Unlike silicon based conventional FETs, contact resistance exists in OFETs, and has a critical contribution to the behavior

of OFET. It is reasonable to conclude that the short-channel effects would be more obvious in OFETs.

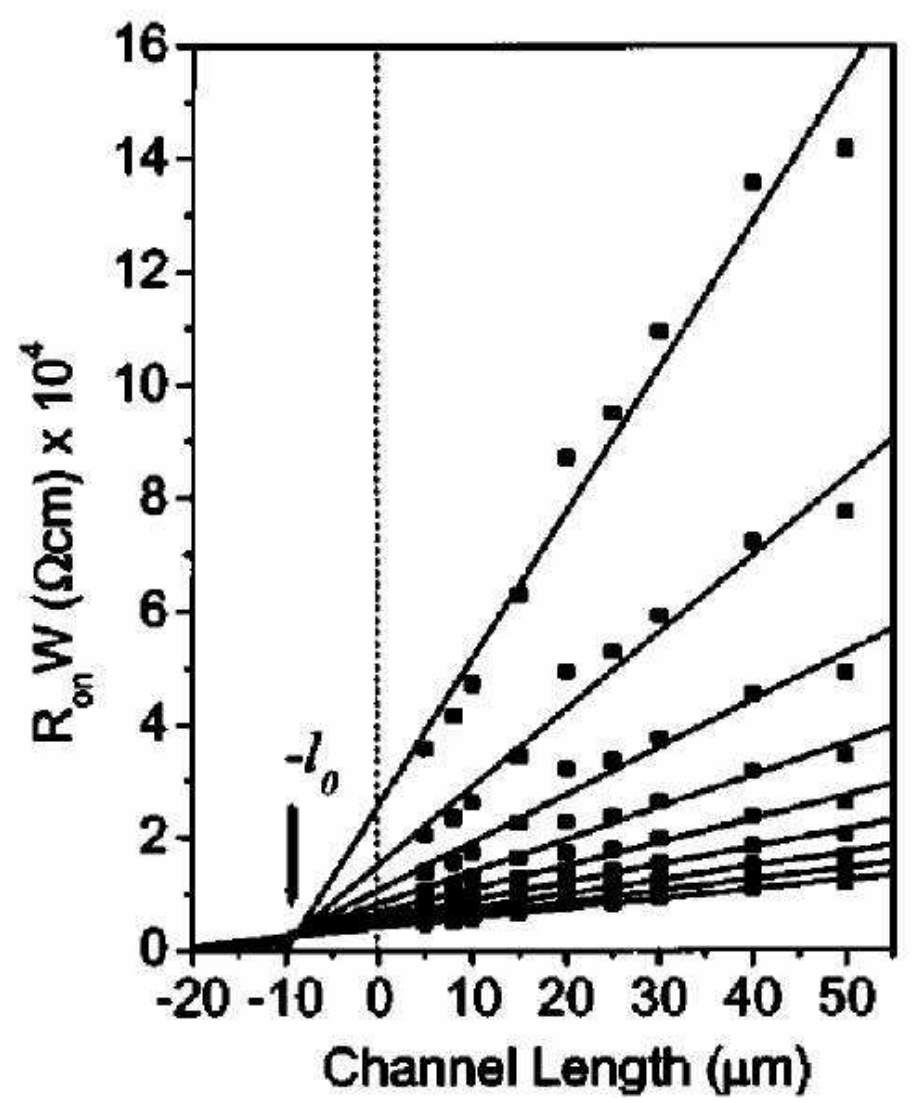


Figure 5.1: Width normalized resistance as a function of channel length at gate voltage from -20 to -100 V, take from[5]

Transfer line method (TLM), which is a classical technique to estimate contact resistance for amorphous silicon thin film transistor, has been used by several groups to investigate contact resistance in OFETs.[5] It consists of measuring the channel length dependent resistance of the device. The contact resistance is extracted by plotting the width-normalized resistance as a function of channel length L. The problem with the TLM is that

it requires measurements on several devices, and it cannot be taken for granted that the contact and channel resistance do not vary from on device to another. So the test results scatter and data are not easy to align during the plotting (Fig 5.1).

The IDS structure discussed in this thesis offers us a good tool to investigate the short-channel effects. The five 4-point-probe units on the IDS chip can provide all the the resistance information for the OFETs with channel length from 10 μm to 200 μm. Based on the design principle, this IDS test platform can be modified to accommodate even smaller scale device and also more devices. On a single casting, we can have several OFETs with different channel length. With the help of auxiliary electrodes, we can use 4-point-probe measurement to calculate the contact resistance at different channel length. Then by plotting the contact resistance versus channel length, we can deduce the pattern of contact resistance changes as function of channel length.

In the previous study, P3HT is deposited on device surface by drop casting because of the leakage problem caused by spin casting. In the study of channel length influence, OS film thickness has to be kept constant among different devices. So spin coating has to be used for creating a uniform OS layer. Several methods can be used to solve the problem. We can either use IDS structure in wafer form instead of dicing it into single chip, then use a probe station to make the measurements. Or we can encapsulate the electro-active edge of the silicon chip with insulating material then do the spin cast. The second method has been tested with several epoxy materials, the size of the chip prevents good encapsulation.

5.2 Develop poly(3-hexylthiophene) based oxygen sensor for application on chemical sensor array

It is a very interesting observation that P3HT can reversibly form charge transfer complex with oxygen, and this reaction is relatively fast. By putting an oxygen barrier on top of P3HT layer, we can control the oxygen diffusion speed. This offers us a good idea of making P3HT based oxygen sensor and incorporate into the chemical sensor array for higher order sensing.

A oxygen barrier layer is very important in developing the oxygen sensor. The barrier layer should be able to control the degradation effect from light, it can be realized by adjusting the light-absorbing additives component in the layer. This layer should also be useful to remove the interferences from the ambient environment. By careful selection of barrier materials, we can control the oxygen doping speed and the reversibility.

We also need to modify the chemical sensor structure. Adding a tiny heater on chip would help to drive the oxygen out of the P3HT sensing layer, then recover the sensor. It is not difficult to add such a heater module in our GT03 design, the only problem would be how to make the heating uniform all over the structure.

The detection of oxygen would be realized by detecting the WF changes in the IGFET configuration or by measuring the impedance change in OFET configuration. Shift of threshold voltage in OFET can also be used for this purpose, but the influence from contact resistance must be considered.

Even though there are already many oxygen sensors on the market, it is still a promising application for the P3HT based oxygen sensor. The small size, higher order sensing and the fast response would be the advantages of this sensor.

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